

South Peak 13" Schematics Document

Tiger LAKE-U 42

2020-10-28

REV: A00

DY : None Installed	TPD4S311 : For using CC protector Installed	SIM: For type C power circuit simplify design
5107 : For MEC5107 Installed	Non-TPD4S311 : For not using CC protector Installed	4G_DY: For 4G cinfig Clip BOM control
5200 : For MEC5200 Installed	1P : 1P Installed	GLUE: WWAN related glue logic
VPRO : VPRO Installed	2P : 2P Installed	NON_GLUE: Stuff when non WWAN glue logic
NON_VPRO : NON_VPRO Installed	WWAN : WWAN Installed	5107_GLUE: WWAN and MEC5107 related glue logic
DDP : For dual die DDR4 Installed	EV_EVT : For EV EVT test Installed	5200_GLUE: WWAN and MEC5200 related glue logic
SDP : For single die DDR4 Installed	DEBUG : For Debug Port Installed	WLAN_CON: For WLAN power enable controll
ONE_CHANNEL : For one channel DDR4 Installed	ST : ST TPM Installed	NON_WLAN_CON: For simplified WLAN power enable controll
TWO_CHANNEL : For two channel DDR4 Installed	NUVOTON : NUVOTON TPM Installed	DY: Do not stuff
BD_BAT : For using Bandon battery Installed	Gen 11 : For Gen 11 OVP Installed	
MX_BAT : For using MX battery Installed	Gen 12 : For Gen 12 OVP Installed	
INT : INT LDO Installed	I5_I7 : For I5_I7 Installed	
EXT : EXT LDO Installed	TEST_RTC : For RTC conn Installed	
EXT_LATCH : For external AC disconnect logic Installed	ORI: For type C power circuit original design	

MULTI BOM

**Wistron Corporation**21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Cover PageSize
A4

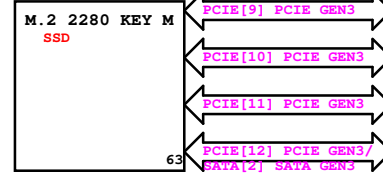
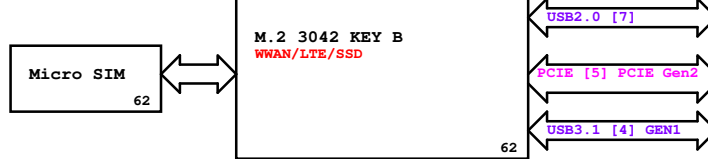
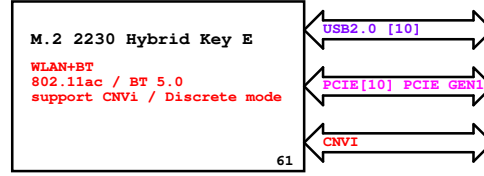
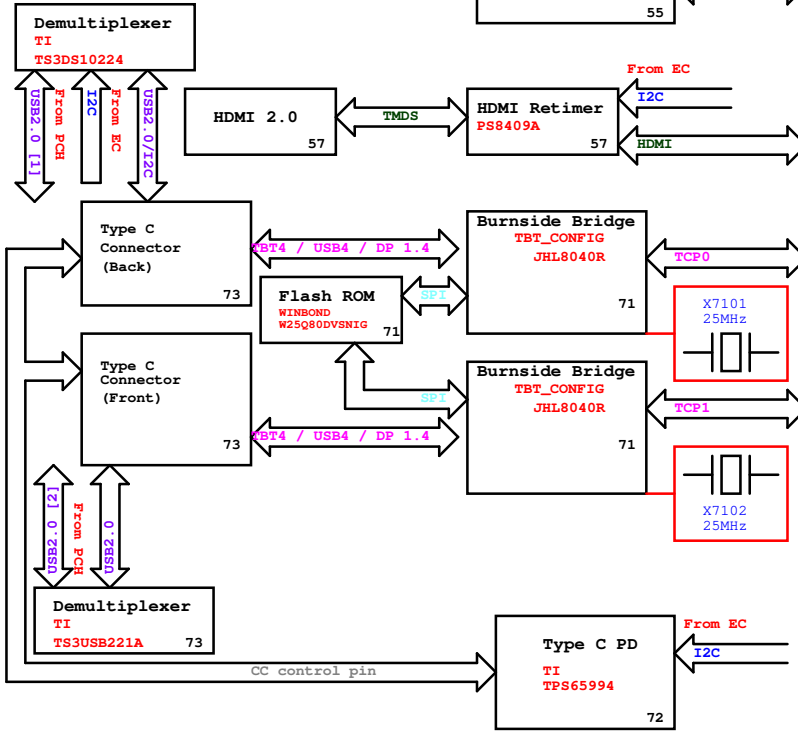
Document Number

SouthPeak13 TGLRev
A00

Date: Wednesday, October 28, 2020

Sheet 1 of 106

Project code : 4PD0M7010001
PCB P/N : 19817
Revision : -1

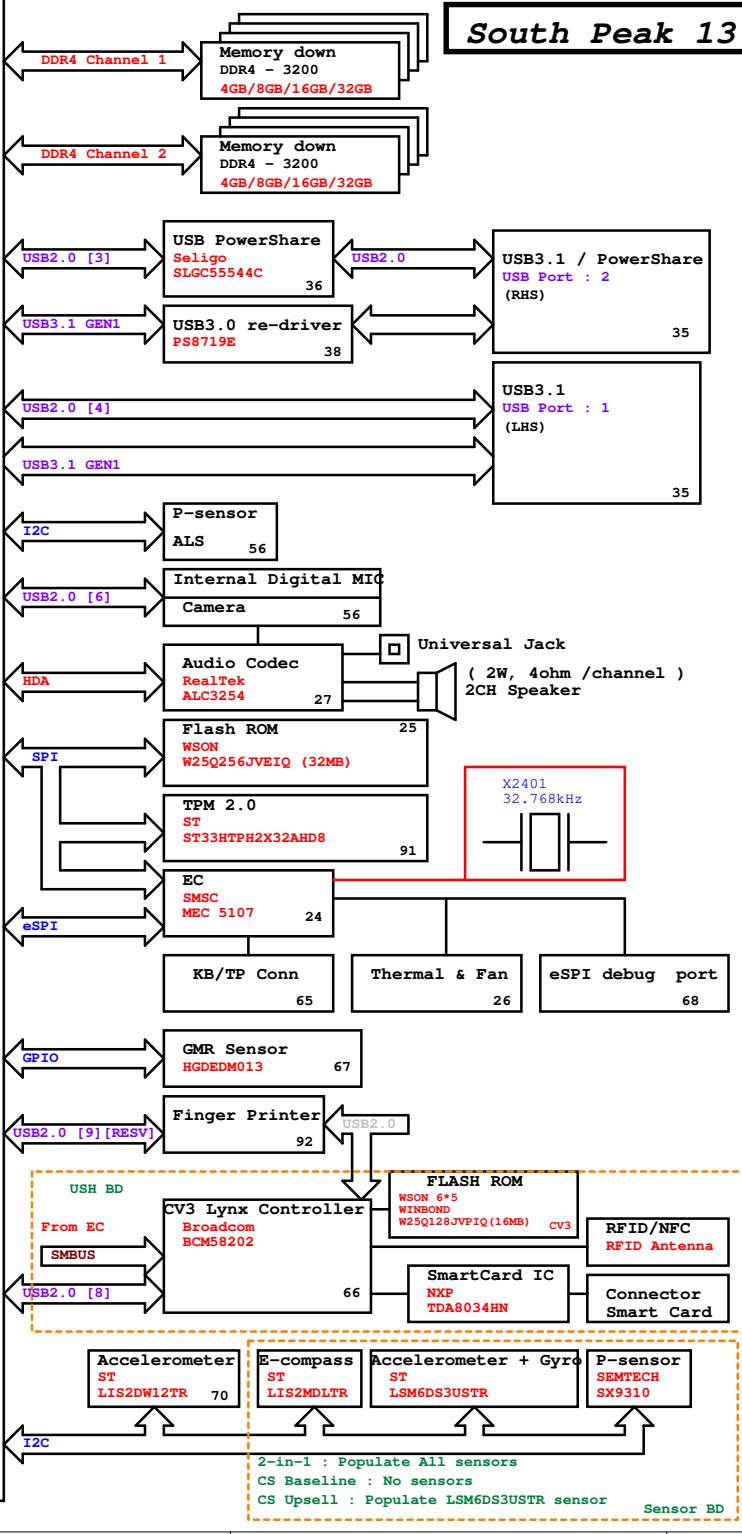


Intel CPU
Tiger LAKE-U 42
TGL U PCH-LP

16 PCIe* Lanes
2 SATA Lanes
4 USB3.1 Gen1/Gen2 Lanes
3 GbE Lanes
2 Remapped PCIe* storage

X1802 32.768kHz
X1803 38.4MHz

3, 4, 5, 6, 7, 8, 9, 10, 11, 15
16, 17, 18, 19, 20, 21, 22, 23



South Peak 13" Block Diagram

https://iinafix.com/	
ISL9538C	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT
SYSTEM DC/DC SY8288BRAC/SY8288CRAC	
45	
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_AUX_S5 5V_S5
CPU DC/DC FDMF3035-GP	
47	
INPUTS	OUTPUTS
DCBATOUT	1V_VCCGT 1V_CPU_CORE
CPU DC/DC ISL95808HRZ-T-1-GP	
50	
INPUTS	OUTPUTS
DCBATOUT	1V_VCCSA
SYSTEM DC/DC SY8288RAC	
51	
INPUTS	OUTPUTS
DCBATOUT	1D2V_S3
SYSTEM DC/DC AOZ2260QI-10-GP	
52	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S5
SYSTEM DC/DC SY8057CQDC	
54	
INPUTS	OUTPUTS
DCBATOUT	1D05V_VCCPRIM_CORE
Load Switches	
INPUTS	OUTPUTS
3D3V_S5	3D3V_S5_PCH 3D3V_LAN 3D3V_S5_WWAN 3D3V_S5_WLAN 2D5V_S3 1D8V_S5 VCDVDD_FUSE 3D3V_S0
3D3V_S0	+3V_AVDD 3D3V_CAMERA_S0 3D3V_S0_SATA
5V_S5	5V_S0 1D05V_VCCIO
5V_S0	+5V_PVDD 5V_TSP_S0 5V_HDMI
1D8V_S5	1D8V_S0
1D2V_S3	0D6V_S0 1D2V_VCCPLL_OC
1D05V_S5	1D05V_VCCST 1D05V_VCCSTG
PCB LAYER (FR4-10 Layer)	
L1:Top L2:GND L3:Signal L4:GND L5:Signal	L6:Signal L7:GND/PWR L8:Signal L9:GND L10:Bottom

MULTIBOM

DELL Wistron Corporation
21F, 8R, Sec.1, Hsin Tai Wu Rd., Hsueh,
Taipei Hsien 221, Taiwan, R.O.C.

File: **SouthPeak13 TGL**

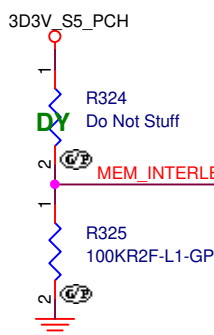
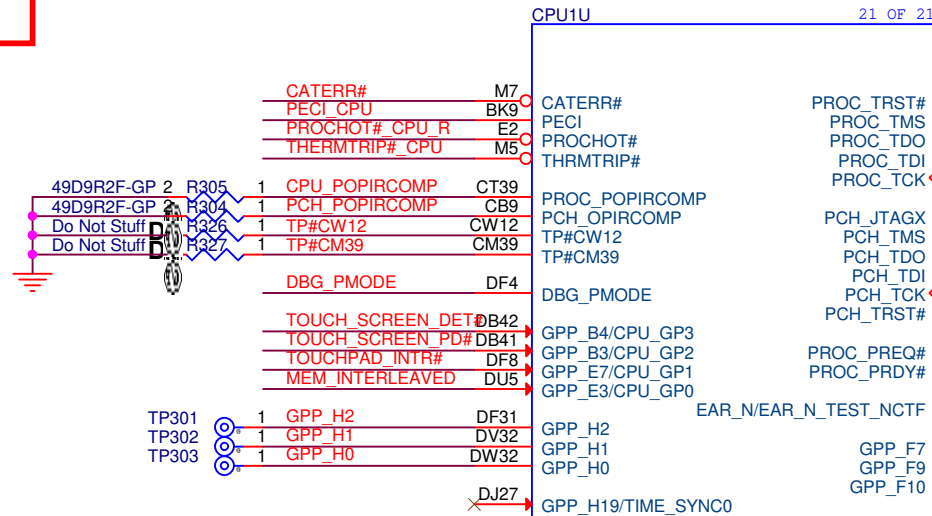
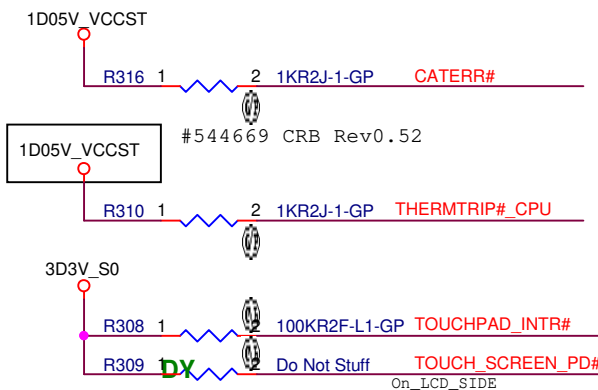
Size: A2 Document Number: Rev: A00

Date: Wednesday, October 28, 2020 Sheet: 2 of 108

Main Func = CPU

[24]	PECI_CPU	<< >>
[22,24]	PROCHOT#_CPU	<< >>
[22,44,46,72,74]	PROCHOT#_PD_R	<< >>
[24]	THERMTRIP#_CPU	<< >>
[6,99]	BPM_N0	<< <
[6,99]	BPM_N1	<< <
[99]	CPU_JTAG_TCK	<< >>
[99]	CPU_JTAG_TDI	<< >>
[99]	CPU_JTAG_TDO	<< >>
[99]	CPU_JTAG_TMS	<< >>
[99]	CPU_JTAG_TRST#	<< >>
[99]	CPU_JTAG_PRDY#	<< >>
[99]	CPU_JTAG_PREQ#	<< >>
[99]	PCH_JTAG_TCK	<< >>
[99]	EAR_N_TEST_NCTF	<< >>
[55]	TOUCH_SCREEN_PD#	>> >
[24,65]	TOUCHPAD_INTR#	>> >
[55]	TOUCH_SCREEN_DET#	>> >
[15,99]	DBG_PMODE	<< <

DIMM_TYPE	
LOW	HIGH
NON_INTERLEAVED	INTERLEAVED



[PECI] and [PROCHOT#]
Impedance control: 50 ohm

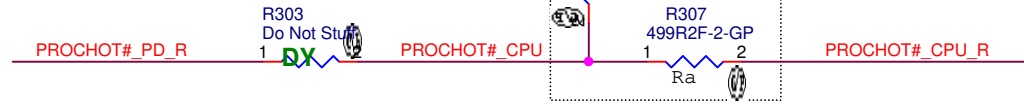
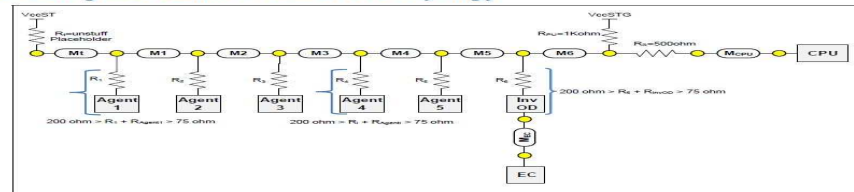
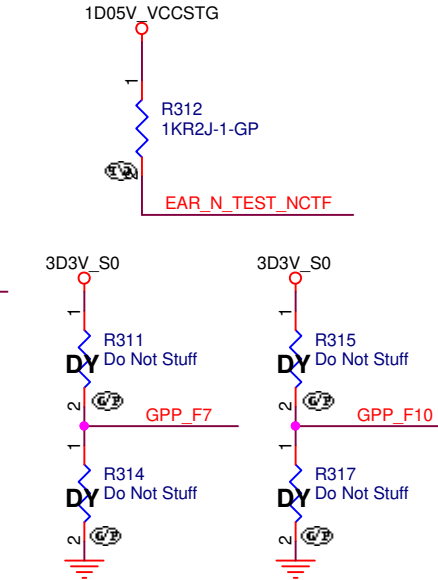
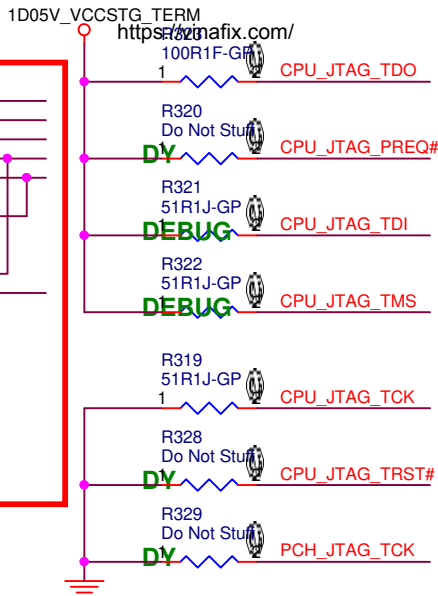
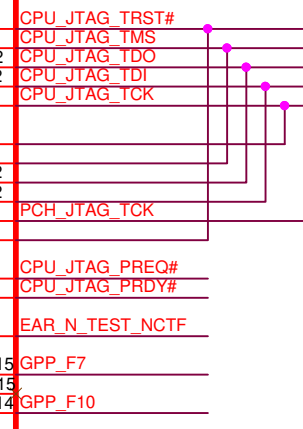


Figure 10-1. Routing Illustration for PROCHOT# Topology



M1,2,3,4,5: <3 inches
M6: 1-11 inches
MCPU: 0.3-1.5 inches
Mt <0.3 mils
Main route (M1+M2+M3+M4+M5+M6+MCPU): 1-12 inches

MIPI



MULTI BOM

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU (THML/JTAG)**

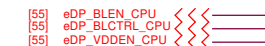
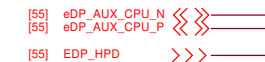
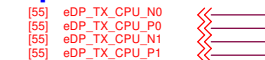
Size A4 Document Number **SouthPeak13 TGL** Rev **A00**

Date: Wednesday, October 28, 2020 Sheet 3 of 106

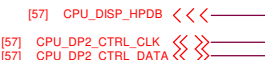
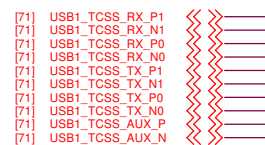
Main Func = CPU

<https://vinafix.com/>

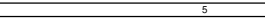
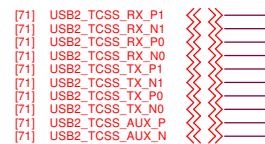
Edp



DP to MUX

**TBT1**

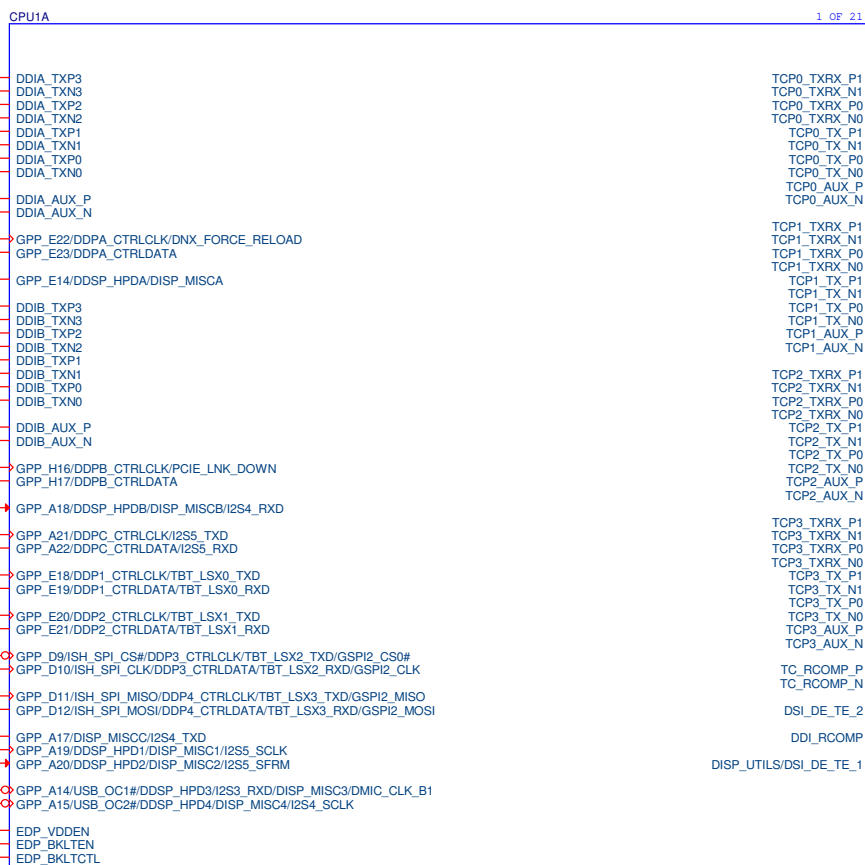
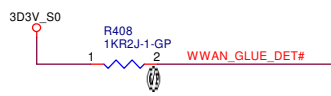
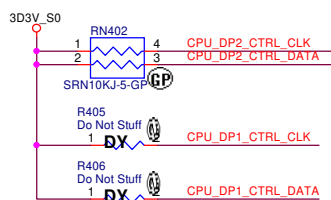
TBT2



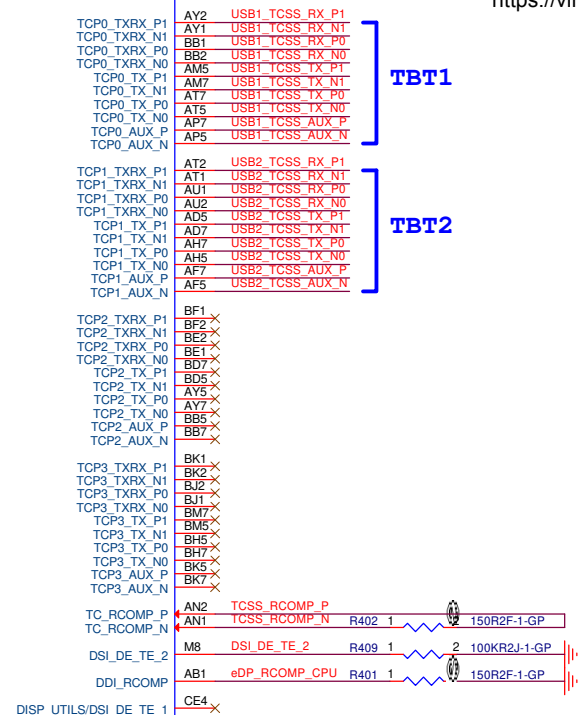
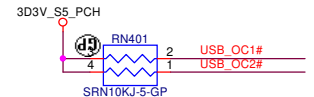
HDMI 2.0

TBT [

TBT2[



Do Not Stuff



MULTI BOM



Title	CPU (DDI/EDP)
-------	----------------------

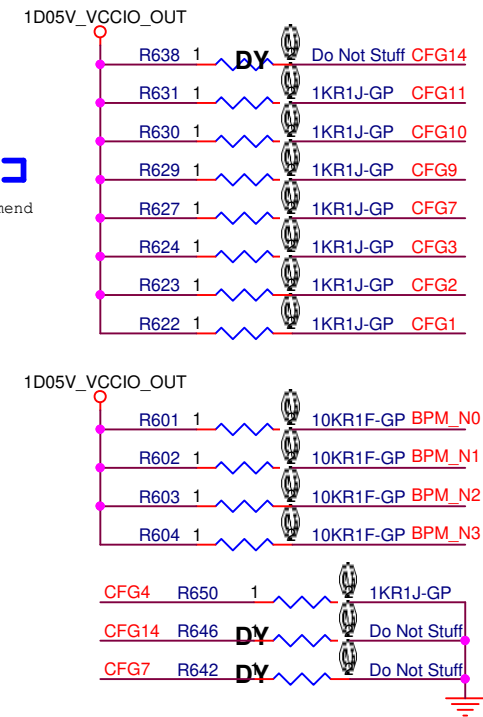
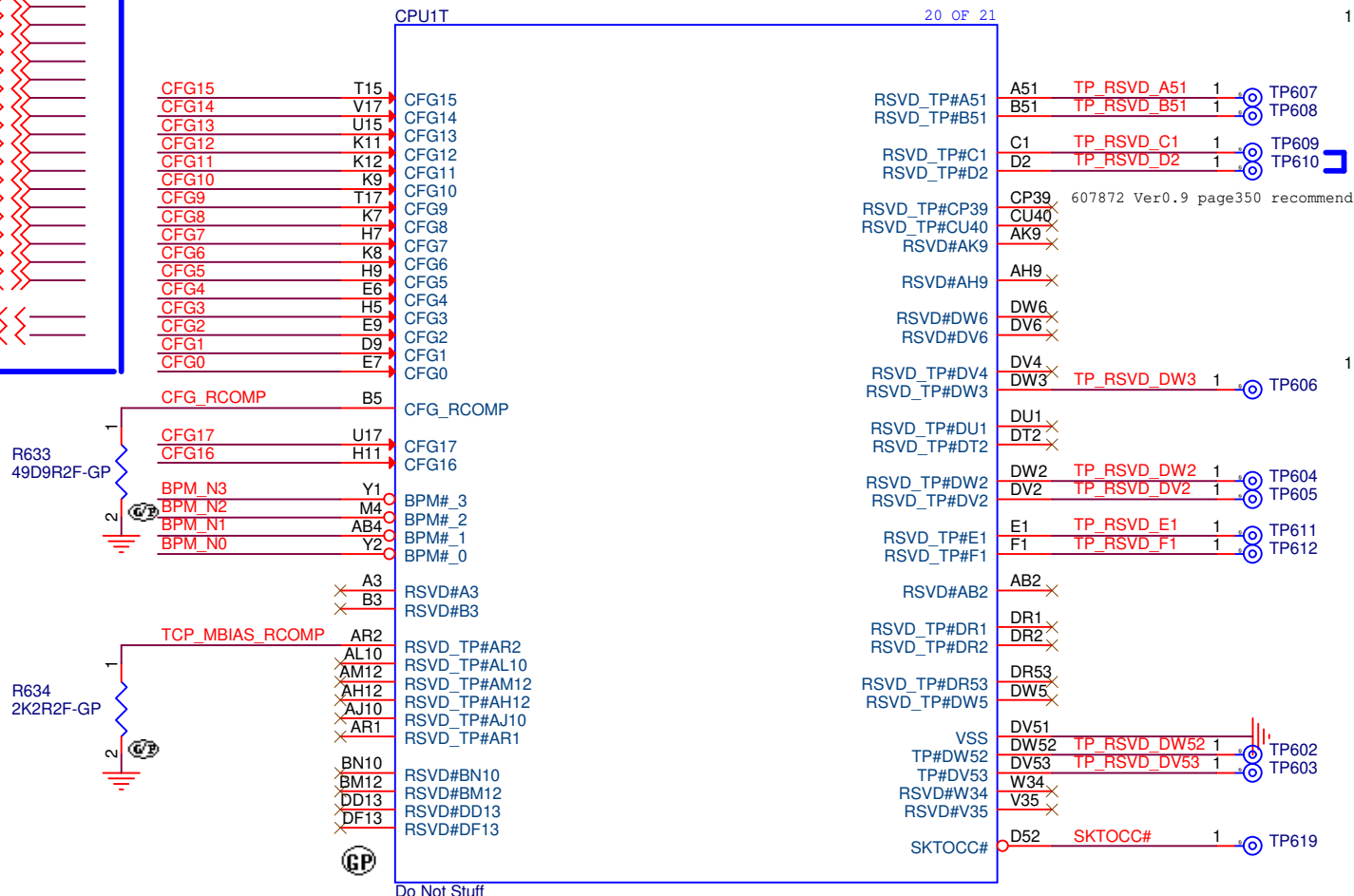
Size A3	Document Number SouthPeak13 TGL	Rev A00
------------	---	------------

Date: Wednesday, October 28, 2020 Sheet 4 of 106

Main Func = CPU

https://vinafix.com/

[99] CFG0
[99] CFG1
[99] CFG2
[99] CFG3
[99] CFG4
[99] CFG5
[99] CFG6
[99] CFG7
[99] CFG8
[99] CFG9
[99] CFG10
[99] CFG11
[99] CFG12
[99] CFG13
[99] CFG14
[99] CFG15
[99] CFG16
[99] CFG17
[99] BPM_N1
[99] BPM_N0



Do Not Stuff
Do Not Stuff

CFG	Description	Termination	Resistor
	Operation; No stall. - 0 = Stall		
CFG[0]	RSVD	None	
CFG[1]	RSVD	Pull-up to VCCIO	1K ohm
CFG[2]	RSVD	Pull-up to VCCIO	1K ohm
CFG[3]	RSVD	Pull-up to VCCIO	1K ohm
CFG[4]	eDP enable Strap: - 1 = Disabled. - 0 = Enabled.	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[6:5]	RSVD	None	
CFG[7]	PEG deferred link training	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[8]	RSVD	None	
CFG[11:9]	RSVD	Pull-up to VCCIO	1K ohm
CFG[13:12]	RSVD	None	
CFG[14]	PEG60 Lane Reversal: - 1 (Default) Normal - 0 - Reversed	Pull-up to VCCIO / Pull-down- Platform design dependent	1K ohm
CFG[1 7:15]	RSVD	None	

MULTI BOM



Title			CPU (CFG/IST)	
Size	Document Number	SouthPeak13 TGL		Rev
A4				A00
Date: Wednesday, October 28, 2020		Sheet 6		of 106

[46] VCCCORE_SENSE <<< —

[46] VSSCORE_SENSE <<< —

[46] SVID_DATA_CPU <<>> —

[46] SVID_CLK_CPU <<>> —

[46] SVID_ALERT#_CPU <<>> —

R703 1 100R2F-L1-GP-U SVID_DATA_CPU
R701 1 56R2J-4-GP SVID_ALERT#_CPU

Layout Note:

C701
Do Not Stuff
DY



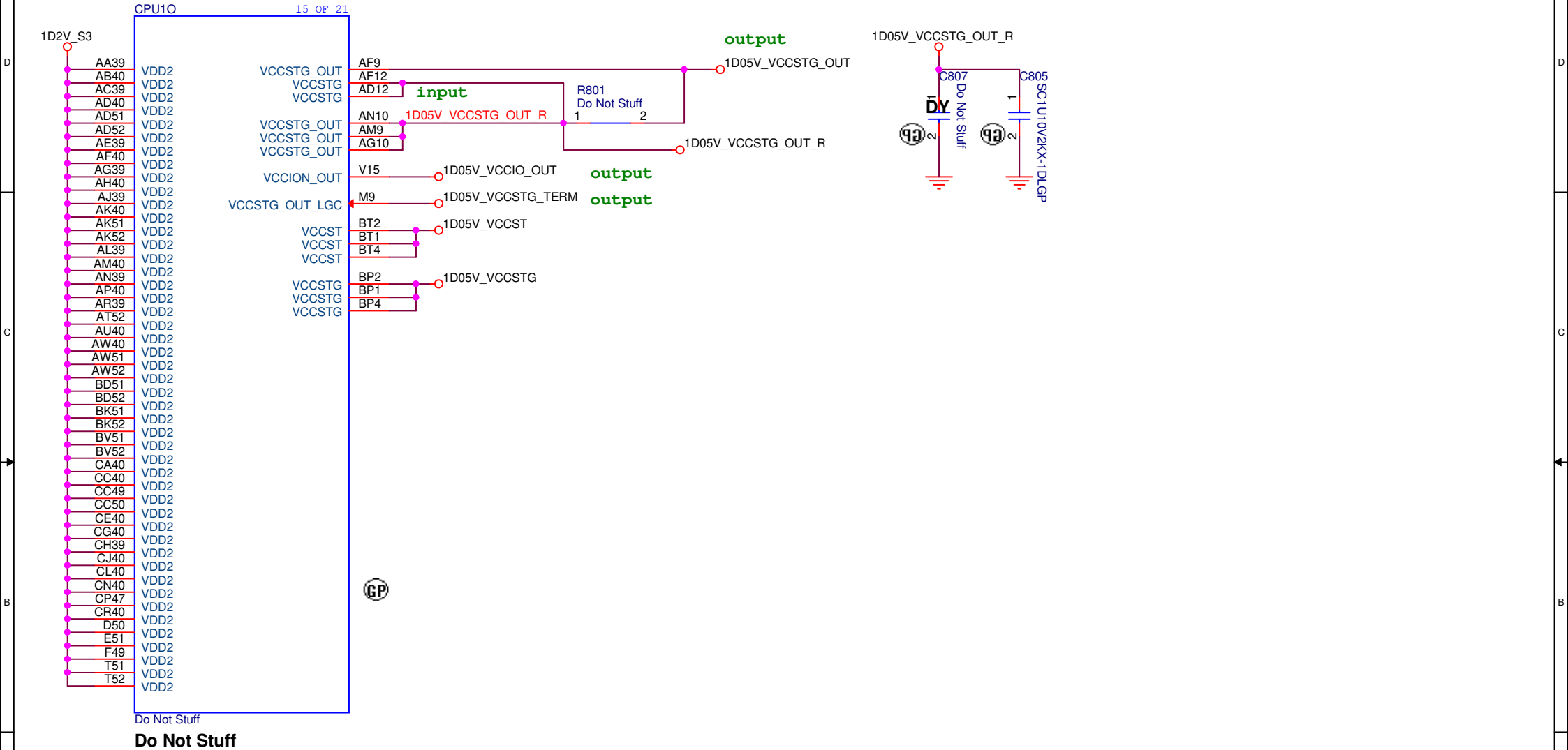
Title	<i>CPU (VCORE/VID)</i>
-------	-------------------------------

Size A4	Document Number SouthPeak13 TGL	Rev A00
------------	---	-------------------


Date: Wednesday, October 28, 2020 Sheet 7 of 106

Main Func = CPU

https://vinafix.com/

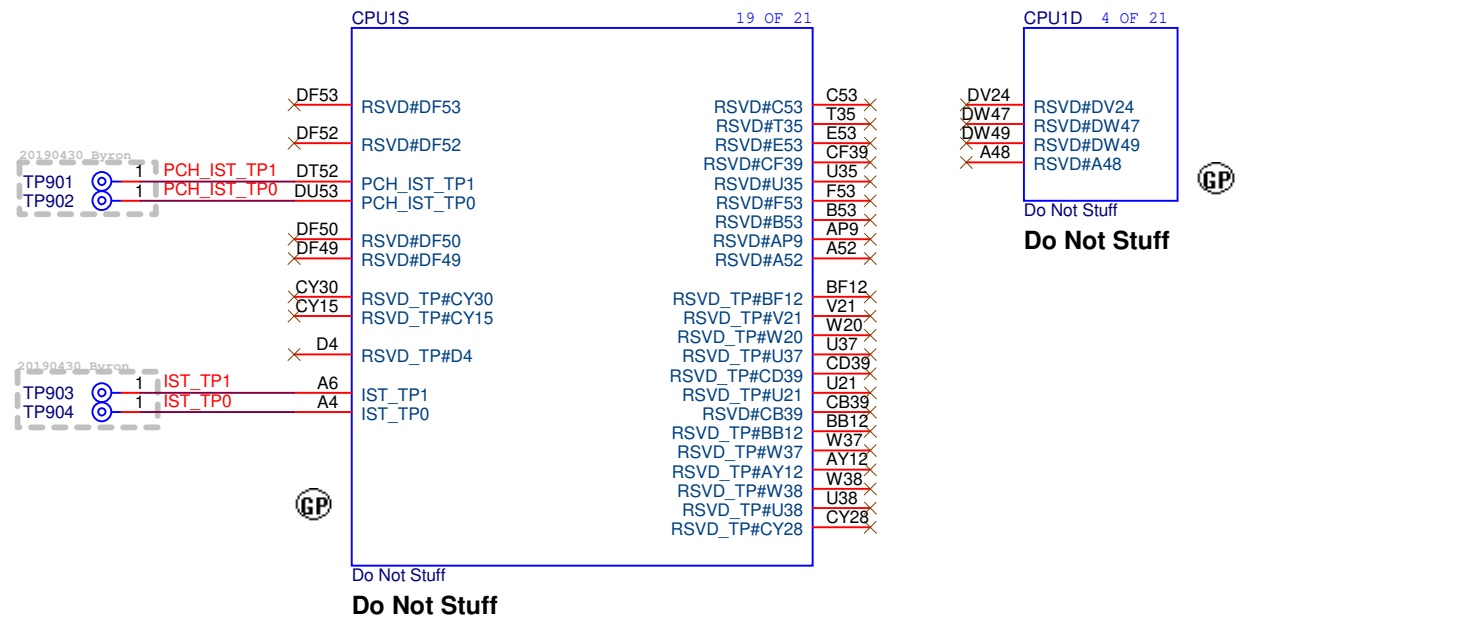


MULTI BOM


			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title CPU (VCCGT/VCCIO/VDDQ/VCCSA)					
Size A4		Document Number SouthPeak13 TGL			Rev A00
Date: Wednesday, October 28, 2020		Sheet 8 of		106	

Main Func = CPU

https://vinafix.com/



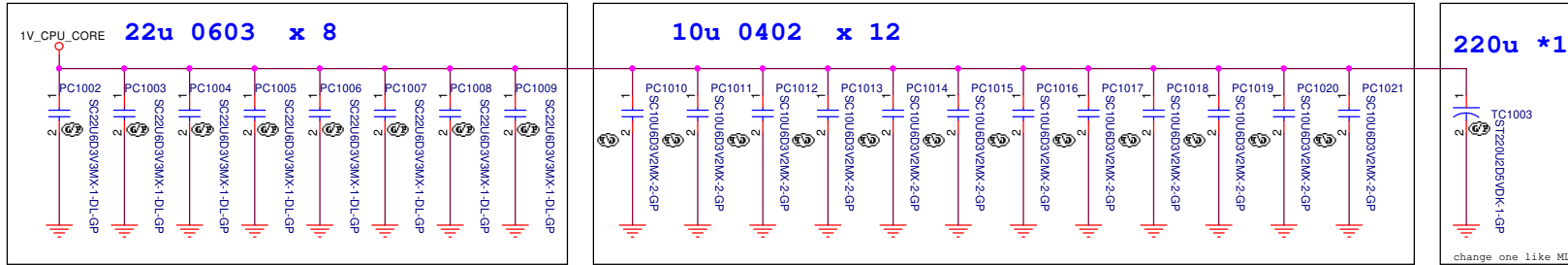
MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
CPU (RSVD)			
Size A4	Document Number SouthPeak13 TGL		Rev A00
Date: Wednesday, October 28, 2020		Sheet 9 of	106

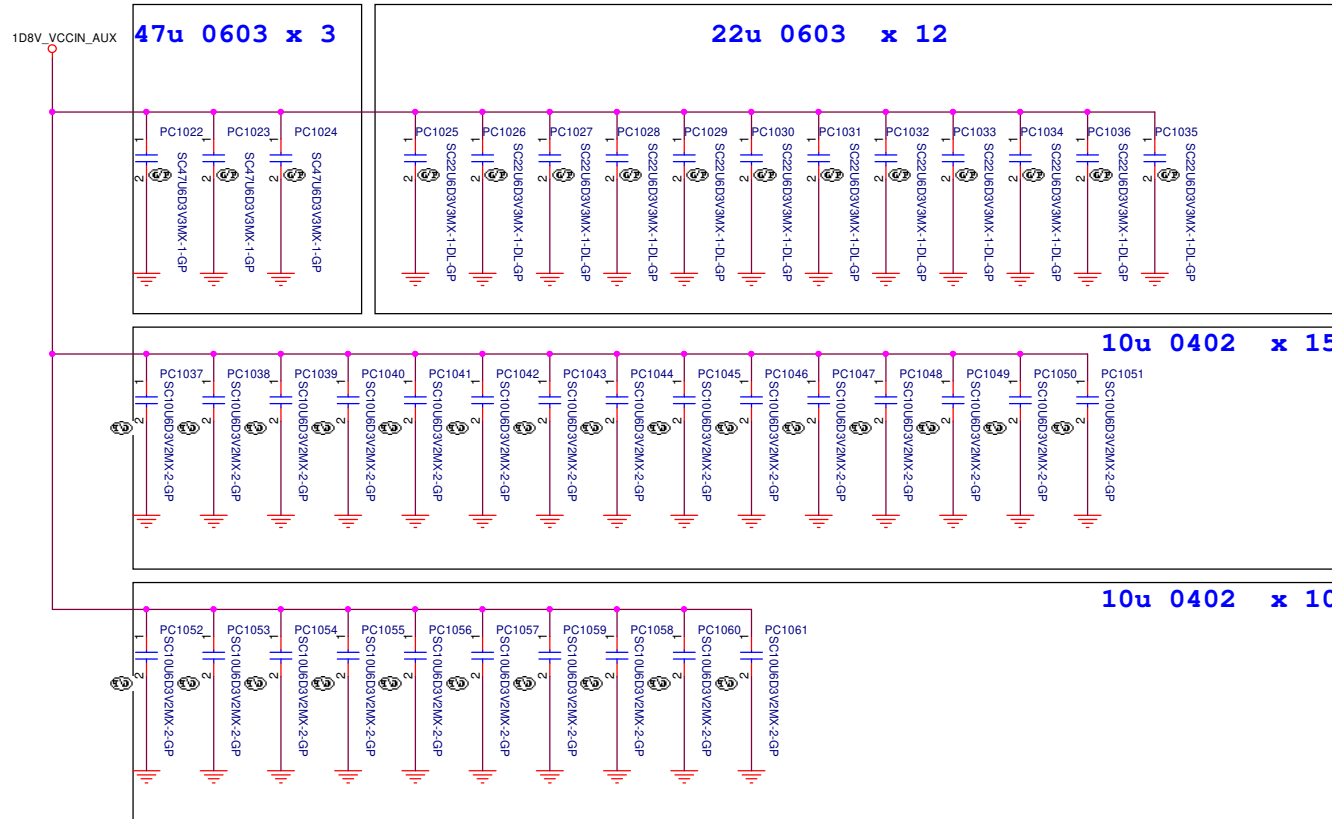
Main Func = CPU

1V_CPU_CORE (VCCIN)

<https://vinafix.com/>



VCCIN_AUX



TGL					
VCCIN	Size.	Value	Uint	Qty	
	0402	10	uF	12	120
	7343	220	uF	2	440
	0603	22	uF	8	176
	7343	Place Holder		2	
				Total	736

VCCIN_AUX	Size.	Value	Uint	Qty	
	7343	220	uF	1	220
	0805	47	uF	3	141
	0603	22	uF	12	264
	0402	10	uF	15	150
	0402	10	uF	10	100
	0805	Placeholder		3	
				Total	875

MULTI BOM

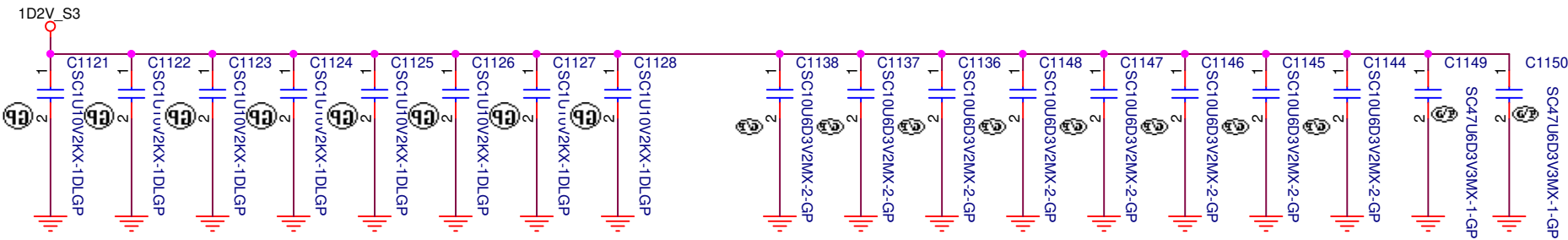


Title	CPU (CORE Power Cap1)		
Size A3	Document Number	SouthPeak13 TGL	Rev A00
Date: Wednesday, October 28, 2020	Sheet 10	of 106	

Main Func = CPU

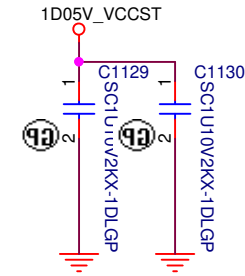
https://vinafix.com/

VDDQ

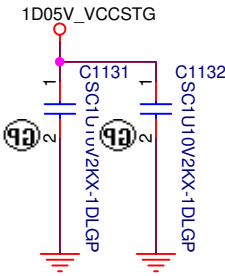


TGL					
VDDQ	Size.	Value	Uint	Qty	
	0603	47	uF	2	94
	0402	10	uF	8	80
	0402	1	uF	8	8
				Total	182

VCCST




VCCSTG



close to CPU side

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (Power Cap2)

Size
A4

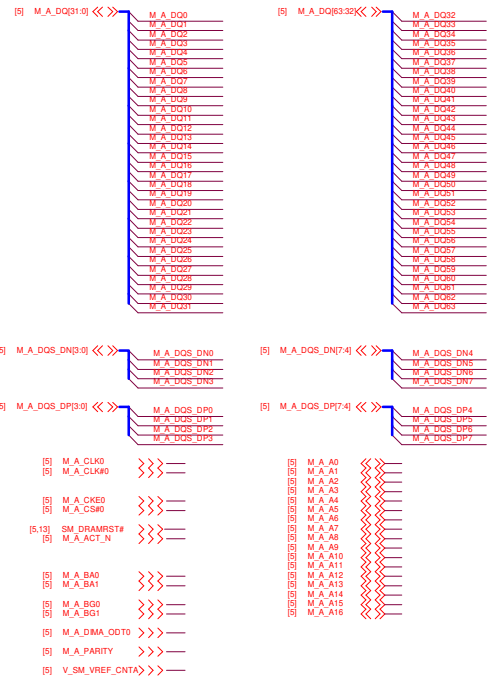
Document Number
SouthPeak13 TGL

Rev
A00

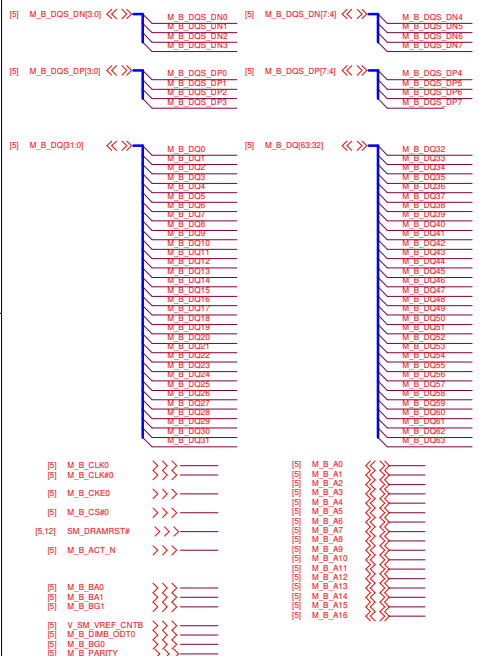
Date: Wednesday, October 28, 2020

Sheet 11 of 106

Main Func = MEMORY

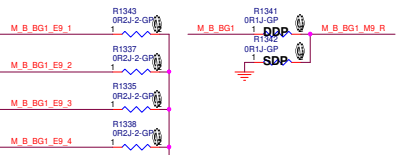


Main Func = MEMORY



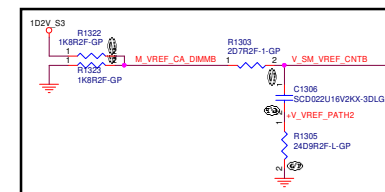
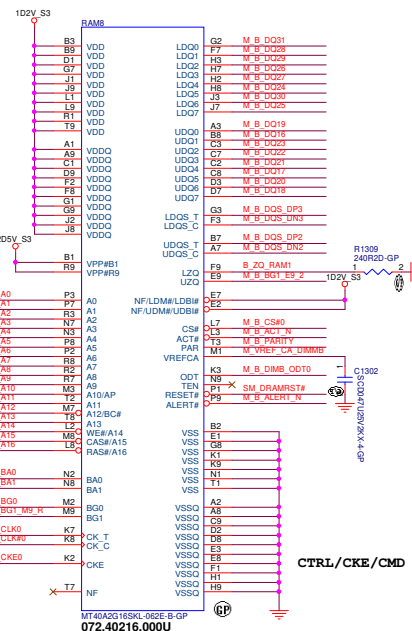
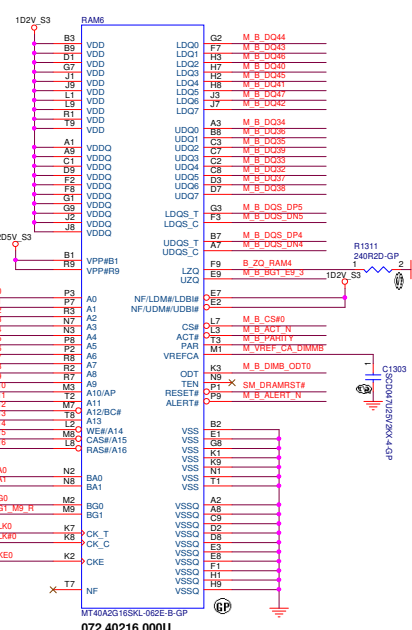
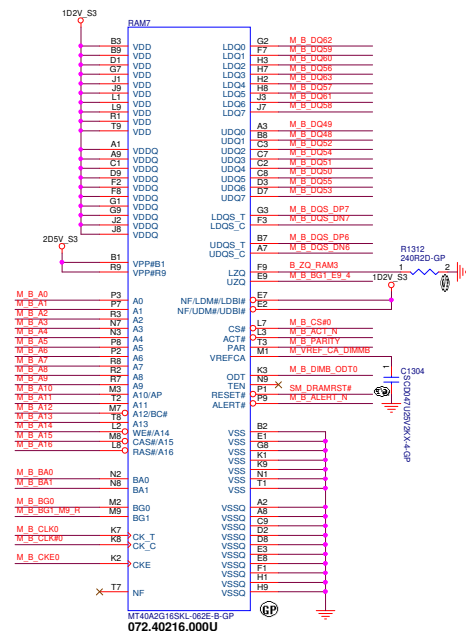
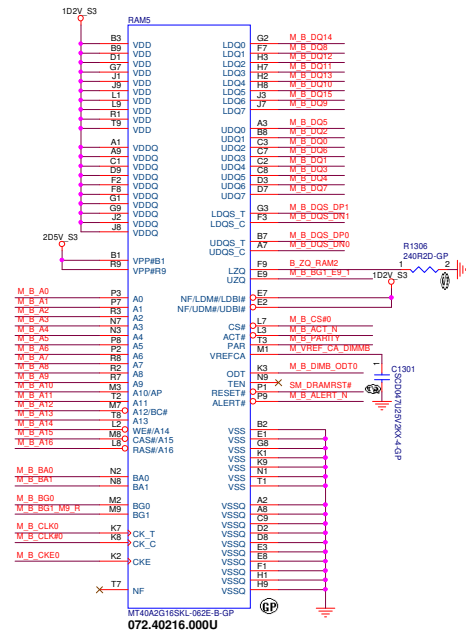
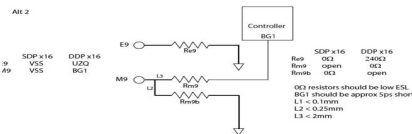
SDP & DDP SETTING

DDP: 240 ohm (64.24005.6DL)
SDP: 0 ohm (63.R0034.1DL)

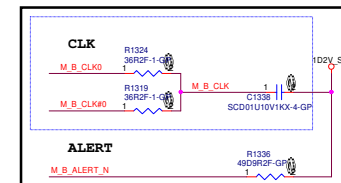


DDP x16 and SDP x16 Compatible Layout

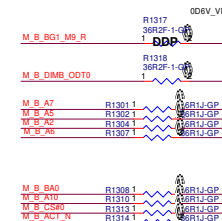
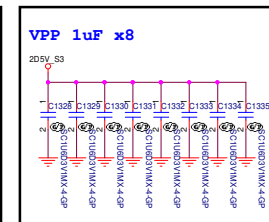
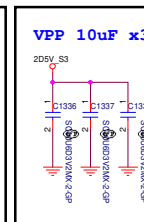
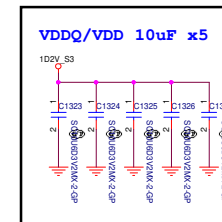
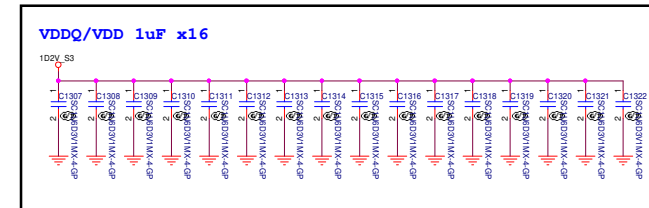
- ▶ Alternate two layout, risk of VSS offset increases a little



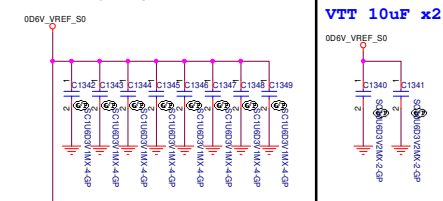
<https://vinafix.com/>



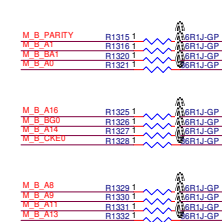
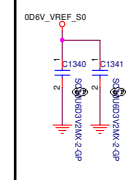
close to cpu



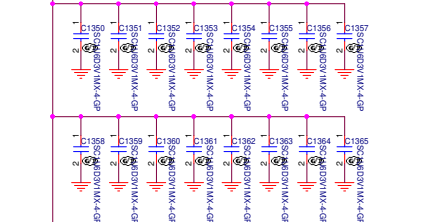
SO



VTT 10uF x2



CTRL/CKE/CMD




Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title			
DDR3-SODIMM1			
Size A2	Document Number	Rev	
	SouthPeak13 TGL	A00	
Date:	Wednesday, October 28, 2020	Sheet	13 of 106

(Blanking)

MULTI BOM

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title DDR (RSVD) (DDR4-CHA1)					
Size A4		Document Number SouthPeak13 TGL			Rev A00
Date: Wednesday, October 28, 2020			Sheet 14 of 106		

Main Func = PCH

- [18,68,99] SPI_SI_CPU <<<—
- [18,68,99] SPI_WP_CPU <<—>
- [18,68] SPI_HOLD_CPU <<—>
- [21,61] CNV_RGL_DT >>—
- [18] GPP_C5 <<<—
- [18] GPP_E6 >>>—
- [19] HDA_SDO <<<—
- [4,71] TBT_LSX0_RXD >>>—
- [4,71] TBT2_LSX0_RXD <<<—
- [3,99] DBG_PMODE <<—>
- [18] GPP_E10 <<—>

GPIO	GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK (GPP_R2)	CNVI debug MODES (GPP_F2)
Schematic							
High	ESPI Disable	Disable	Enable	19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL)	Disable	OVERRIDEN	INTEGRATED CNVI DISABLE
Low	Enable =default=	Enable	Disable	38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT)	Enable	SECURITY MEASURES NOT OVERRIDEN	INTEGRATED CNVI ENABLE
GPIO	TBT LSX VCCIO conf. #0	TBT LSX VCCIO conf. #1	TBT LSX VCCIO conf. #2	TBT LSX VCCIO conf. #3	A0		GPP_E10
Schematic							
High	3.3V	3.3V	3.3V	3.3V	Disable	DFXTESTMODE DISABLED (DEFAULT)	
Low	1.8V	1.8V	1.8V	1.8V	Enable	DFXTESTMODE ENABLED	

Original Ref.

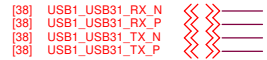
GPP_C5	SPI_SI	GPP_E6	GPP_B23	SPI_WP	ME_UNLOCK	M.2 CNVI MODES	TBT LSX #0
ESPI OR EC LESS HIGH: ESPI IS DISABLED LOW: ESPI SELECTED WEAK INTERNAL PD 20K	BOOT HALT HIGH: -DISABLED LOW: ENABLED NO INTERNAL PUPD	JTAG ODT DISABLE LOW: JTAG ODT DISABLED HIGH: JTAG ODT ENABLED NO INTERNAL PUPD	CPUSSC CLOCK FREQ HIGH: 19.2MHZ CLOCK FROM DIVIDER (DERIVED FROM 38.4MHZ CRYSTAL) LOW: 38.4MHZ CLOCK FROM DIRECT CRYSTAL (DEFAULT) WEAK INTERNAL PD 20K	CONSENT STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PU/PD	FLASH DESKTOP/PC SECURITY OVERRIDE HIGH: OVERRIDEN LOW: SECURITY MEASURES NOT OVERRIDEN WEAK INTERNAL PD 20K	M.2 CNVI MODES LOW-> INTEGRATED CNVI ENABLE HIGH-> INTEGRATED CNVI DISABLE NO INTERNAL PUPD	TBT LSX #0 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD
TBT LSX #1	TBT LSX #2	TBT LSX #3	A0	GPP_E10	GPP_E11		
TBT LSX #1 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	TBT LSX #2 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	TBT LSX #3 PINS VCCIO CONFIGURATION HIGH: 3.3V LOW: 1.8V NO INTERNAL PUPD	A0 PERSONALITY STRAP HIGH: DISABLED LOW: ENABLED NO INTERNAL PUPD				

https://vinafix.com/

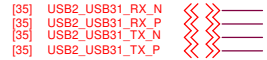
MULTI BOM

Main Func = PCH

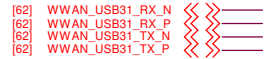
USB3.1 PORT1



USB3.1 PORT2



WWAN



FP



CARD



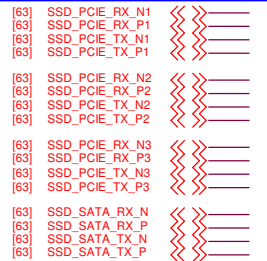
WLAN



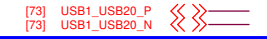
WWAN



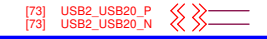
SSD



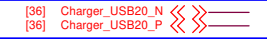
Type C port 1



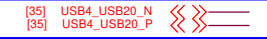
Type C port 2



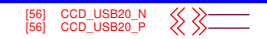
USB charger



USB2.0 port4



CAMERA



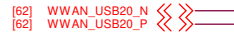
#543016:
220 nF nominal capacitors are recommended for Gen 3.
100 nF nominal capacitors are recommended for Gen 2.

(#545659) The xHCI controller supports USB Debug port on all USB3.0 capable ports.

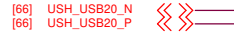
<https://vinafix.com/>

SSD

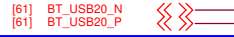
WWAN



USH



BT



CARDREADER

WLAN

WWAN

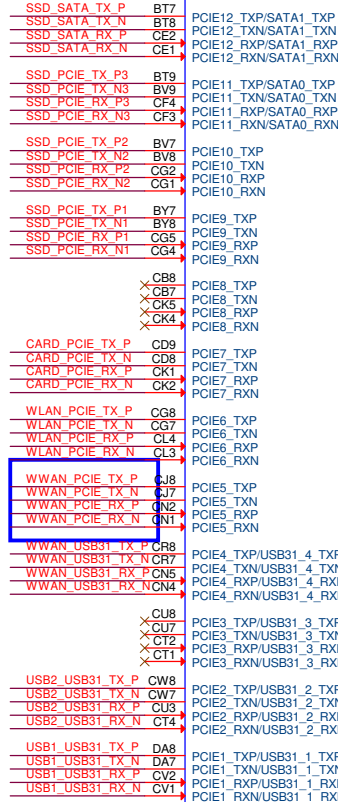
WWAN

USB4 Type A port2

USB3 Type A port1

CPU11

9 OF 21



Do Not Stuff

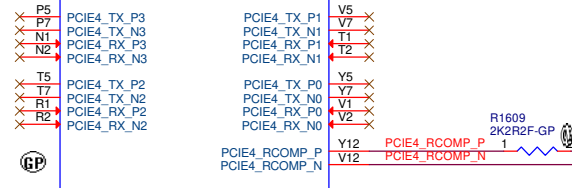
Do Not Stuff

Layout Note:

- Trace Width: 4 mils min (breakout) 12-15 mils (trace)
Note: Must maintain low DC resistance routing (<0.1 ohm).
- Isolation Spacing: At least 12 mils to any adjacent high speed I/O.

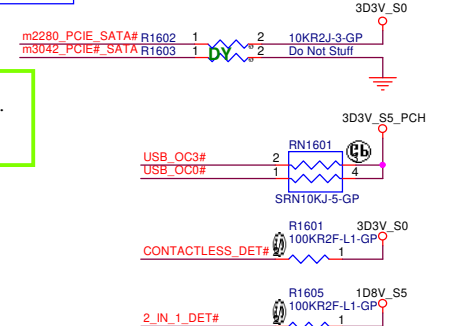
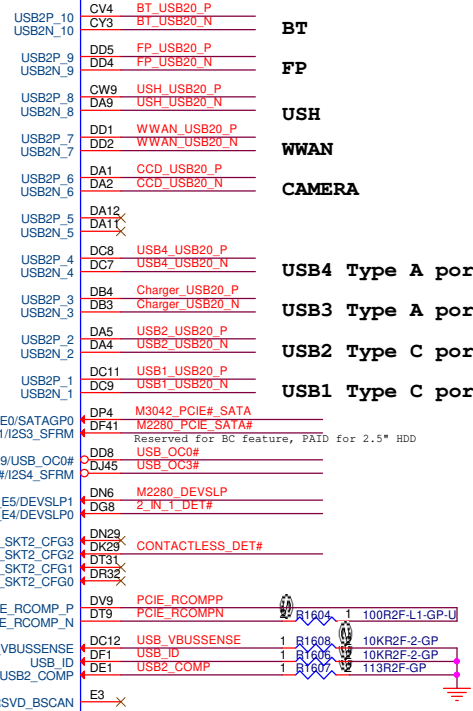
CPU1H

8 OF 21




Do Not Stuff

Do Not Stuff



MULTI BOM

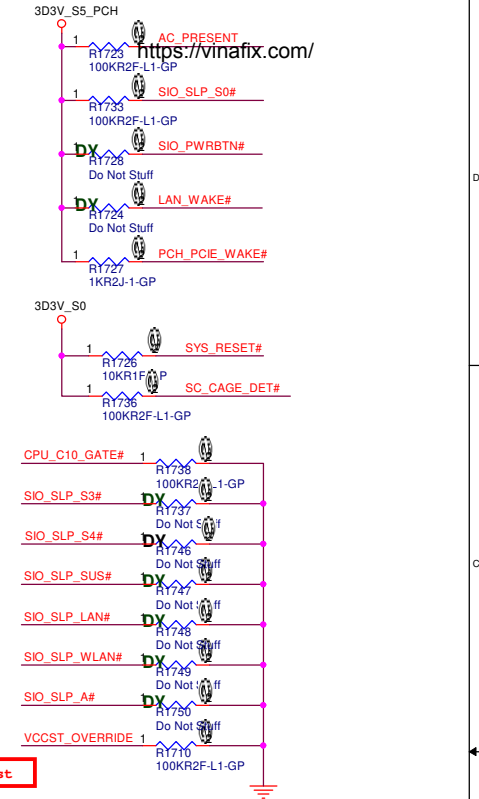
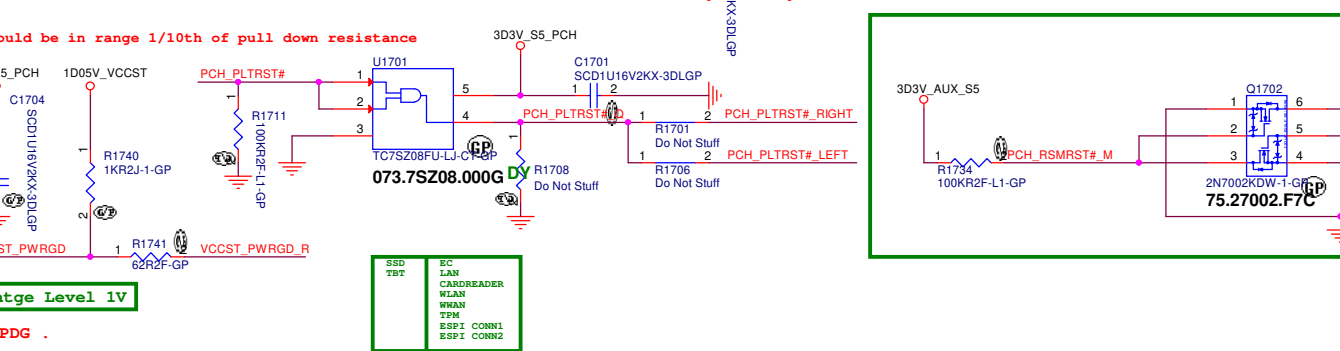
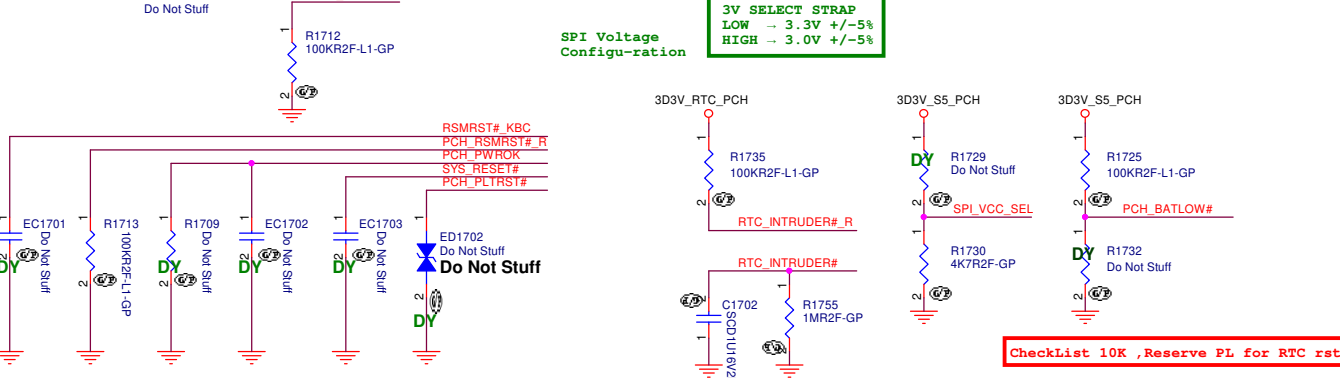
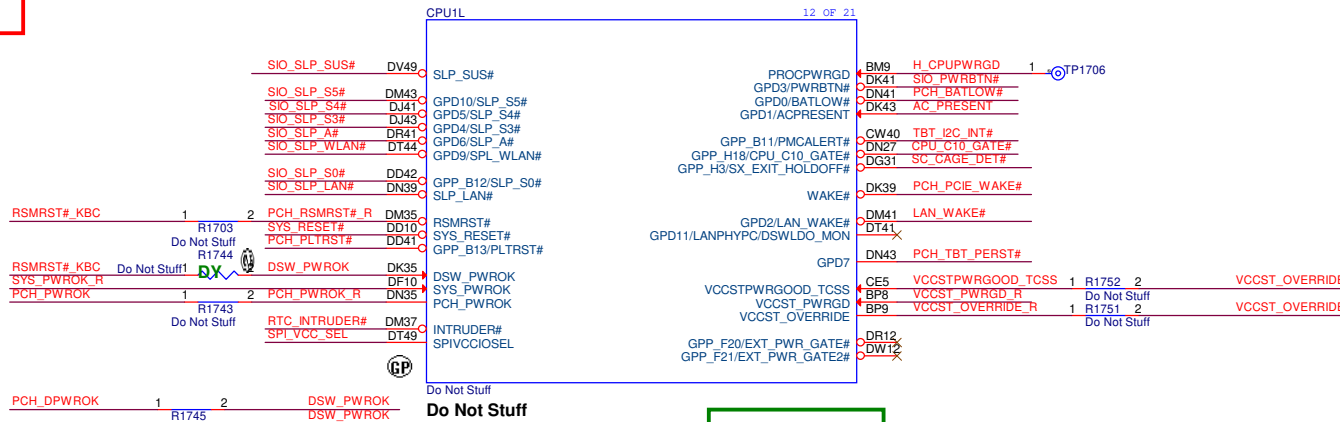


Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		CPU (PCIE/SATA/USB)	
Size	Document Number	SouthPeak13 TGL	
A3		Rev	A00
Date: Wednesday, October 28, 2020		Sheet	16 of 106

Main Func = PCH

[24,53]	SIO_SLP_SUS#	<<<
[68]	SIO_SLP_S5#	<<<
[51,68]	SIO_SLP_S4#	<<<
[24,40,68]	SIO_SLP_S3#	<<<
[68]	SIO_SLP_A#	<<<
[68,91]	SIO_SLP_S0#	<<<
[68,99]	SYS_RESET#	<<<
[44,46]	PCH_PWROK	>>>
[24]	SYS_PWROK_R	>>>
[24,99]	SIO_PWRBTN#	>>>
[24]	AC_PRESENT	<<<
[24,62]	PCH_PCIE_WAKE#	<<<
[24]	PCH_DPWROK	>>>
[18,24]	RTCST_ON	>>>
[24,64,99]	RSMRST#_KBC	>>>
[24]	ALL_SYS_PWRGD	>>>
[33,61,62,91]	PCH_PLTRST#_RIGHT	<<<
[63,71]	PCH_PLTRST#_LEFT	<<<
[40,91]	CPU_C10_GATE#	<<<
[44]	AC_DIS_ACP	>>>
[40]	VCCST_OVERRIDE	<<<
[72]	TBT_I2C_INT#	>>>
[71]	PCH_TBT_PERST#	>>>
[89]	RTC_INTRUDER#	>>>
[89]	RTC_INTRUDER#_R	>>>
[66]	SC_CAGE_DET#	<<<





SPI ROM					
[68]	SPI_CLK_CPU	↗	↗	↗	—
[15,68,99]	SPI_SI_CPU	↗	↗	↗	—
[68]	SPI_SO_CPU	↗	↗	↗	—
[15,68,99]	SPI_WP_CPU	↗	↗	↗	—
[15,68]	SPI_HOLD_CPU	↗	↗	↗	—
[68]	SPI_CS_CPU_N0	↗	↗	↗	—
[68]	SPI_CS_CPU_N1	↗	↗	↗	—
[91]	SPI_CS_CPU_N2	↗	↗	↗	—

WLAN

[61]	WLAN_CLK_CPU_P	⚡⚡⚡	_____
[61]	WLAN_CLK_CPU_N	⚡⚡⚡	_____
[61]	WLAN_CLKREQ_CPU_N	⚡⚡⚡	_____

WWAN	[62]	WWAN_CLK_CPU_P	<<<	_____
	[62]	WWAN_CLK_CPU_N	<<<	_____
	[62]	WWAN_CLKREQ_CPU_N	<<<	_____

[15] GPP_E6

[15] GPP_E10  

CARD

[33]	CARD_CLK_CPU_N	↔↔↔
[33]	CARD_CLK_CPU_P	↔↔↔
[33]	CARD_CLKREQ_CPU_N	↔↔↔

SSD

[63]	SSD_CLK_CPU_N	⋈⋈⋈	—
[63]	SSD_CLK_CPU_P	⋈⋈⋈	—
[63]	SSD_CLKREQ_CPU_N	⋈⋈⋈	—

ESPI	[24:68]	ESPI_I00	<<	>>	_____
	[24:68]	ESPI_I01	~~~~~	~~~~~	_____
	[24:68]	ESPI_I02	~~~~~	~~~~~	_____
	[24:68]	ESPI_I03	~~~~~	~~~~~	_____
	[24:68]	ESPI_CS#	~~~~~	~~~~~	_____
	[24:68]	ESPI_RESET#	~~~~~	~~~~~	_____
	[24:68]	ESPI_CLK	~~~~~	~~~~~	_____
	[24:68]	ESPI_CLK_RR	~~~~~	~~~~~	_____

OTHER

[99]	CPU_SMB_SCL_DDR	<<<>>>	_____
[99]	CPU_SMB_SDA_DDR	<<<>>>	_____

[71]	SML0_SMBCLK	《》	—
[71]	SML0_SMBDATA	《》	—
[72]	SML1_SMBCLK	《》	—
[72]	SML1_SMBDATA	《》	—

[15] GPP_C5 <<< —

[61,63] SUSCLK <<< —

```
[62] WWAN_GPIO_PERST# <<< _____
[62] WWAN_BB_RST# <<<< _____
[62] WWAN_GPIO_WAKE# <<<<< _____
```

[55]	TS_INT#	<<< —
[57]	HDMI_PD#	<<<

[61] CL_CLK
[61] CL_RST#
[61] CL_DATA

```
[68] RTC_RST#      <<< _____
[56] SECURE_BIO     <<< _____
```

```
[24]  RTCRST_ON      >>>_____
[33]  MEDIACARD_IRQ#  <<<_____
```

```
[25] RTC_DET#          >>>_____
[56] CAM_MIC_CBL_DET#   >>>_____
```

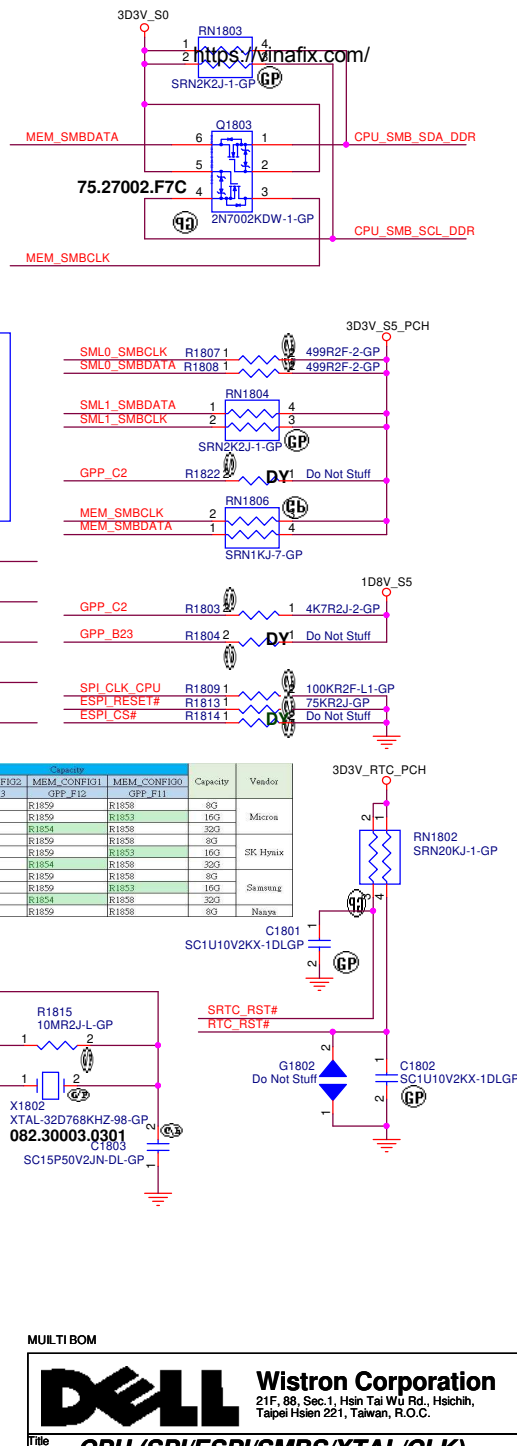
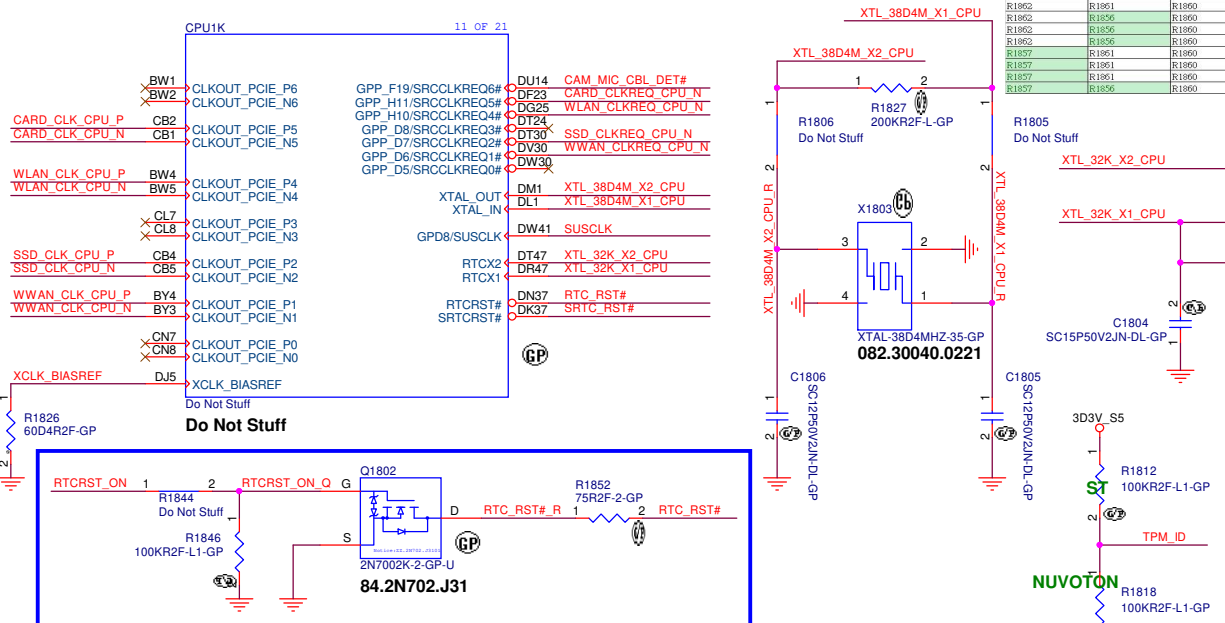
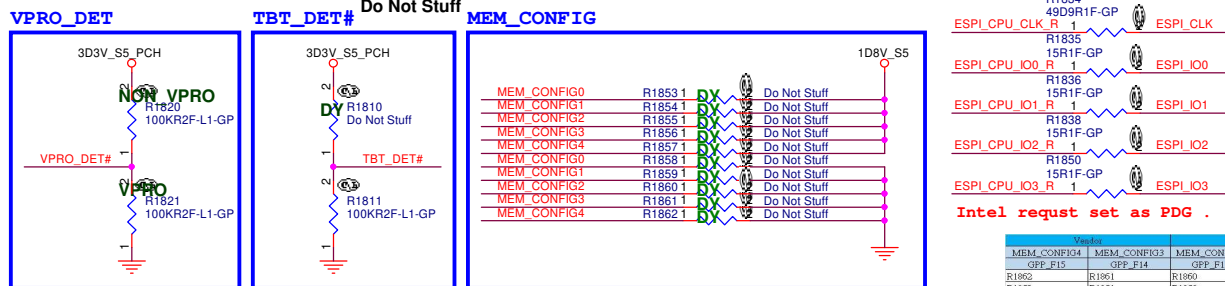
3D3V_S0

1	8	CARD_CLKREQ_CPU_N
2	7	WWAN_CLKREQ_CPU_N
3	6	WLAN_CLKREQ_CPU_N
4	5	SSD_CLKREQ_CPU_N

R1829 1 SRN20KJ GP 2 SECURE_BIO

SUSCLK R1817 1 **DX** 2 Do Not Stuff

3D3V_S0
R1816 1 100KR2F-L1-GP CAM_MIC_CBL_DE



Vendor		Capacity					Vendor
MEM_CONF04 GFF F15	MEM_CONF03 GFF F14	MEM_CONF02 GFF F13	MEM_CONF01 GFF F12	MEM_CONF00 GFF F11	Capacity		
R1862	R1861	R1860	R1859	R1858	80	Micron	
R1862	R1861	R1860	R1859	R1853	16G		
R1862	R1861	R1860	R1854	R1858	32G		
R1862	R1856	R1860	R1858	R1858	80	SK Hynix	
R1862	R1856	R1860	R1859	R1853	16G		
R1862	R1856	R1860	R1854	R1858	32G		
R1857	R1861	R1860	R1859	R1858	8G	Samsung	
R1857	R1861	R1860	R1859	R1853	16G		
R1857	R1861	R1860	R1854	R1858	32G		
R1857	R1856	R1860	R1858	R1858	80		
						Nanya	

MULTI BOM



Title **CPU (SPI/ESPI/SMBS/XTAL/CLK)**

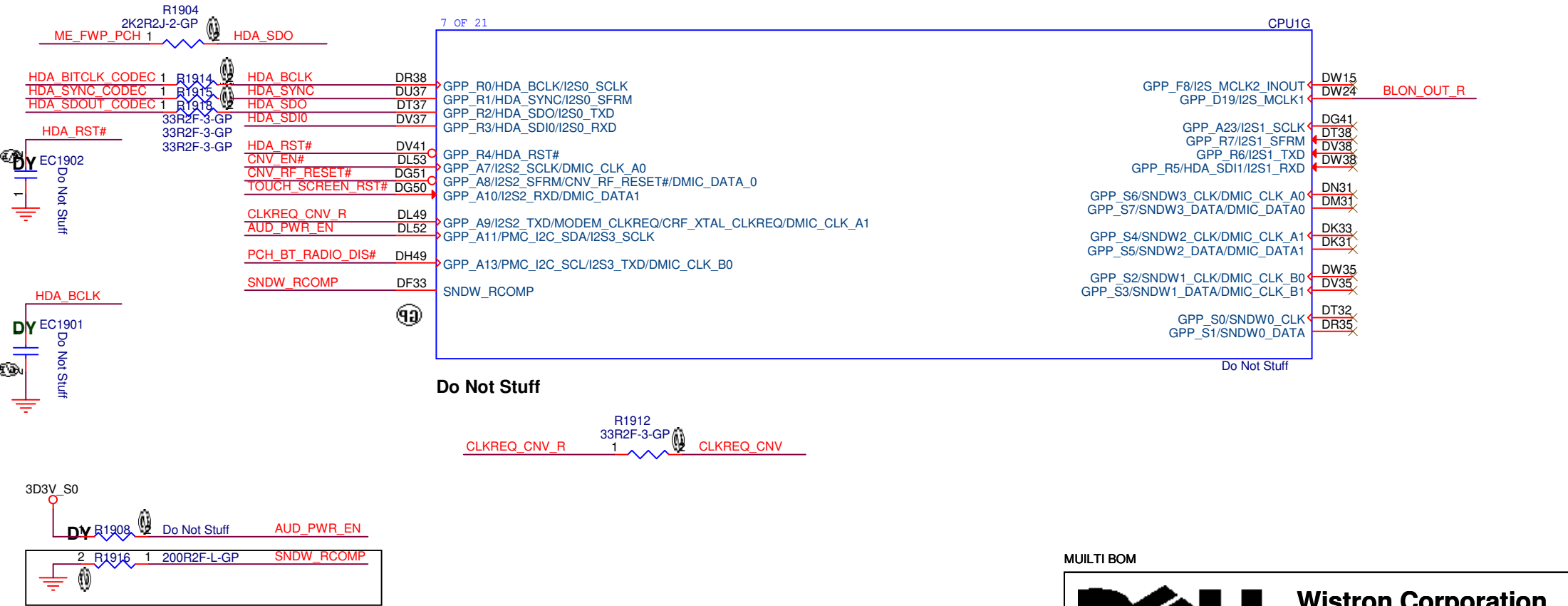
Size A3	Document Number SouthPeak13 TGL	Rev 100
------------	---	------------

Date: Wednesday, October 28, 2020 Sheet 18 of 106


Main Func = PCH

https://vinafix.com/

[27]	HDA_SDIO	<<<	---
[27]	HDA_SDO	<<<	---
[27]	HDA_SYNC	<<<	---
[27]	HDA_BITCLK	<<<	---
[15]	HDA_RST#	<<<	---
[55]	TOUCH_SCREEN_RST#	<<<	---
[68]	ME_FWP_PCH	<<<	---
[61]	CNV_EN#	<<<	---
[61]	CLKREQ_CNV	<<<	---
[61]	CNV_RF_RESET#	<<<	---
[61]	PCH_BT_RADIO_DIS#	<<<	---
[55]	BLON_OUT_R	>>>	---



MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (HDA/I2S/SD/DMIC)

Size
A4

Document Number
SouthPeak13 TGL

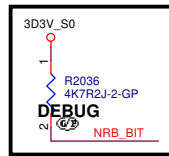
Rev
A00

Date: Wednesday, October 28, 2020

Sheet 19 of 106

Main Func = PCH

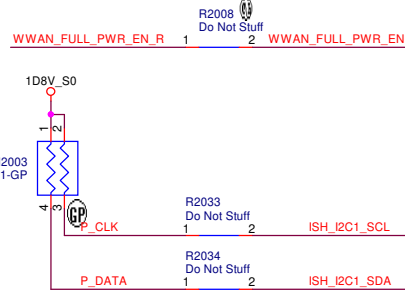
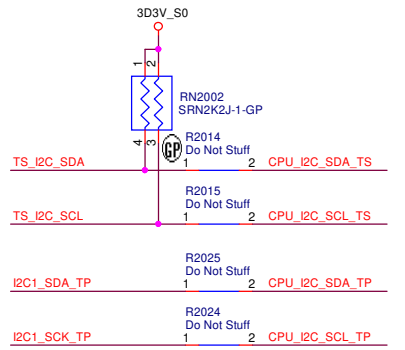
[68]	CPU_UART2_TXD	<<<
[68]	CPU_UART2_RXD	<<<
[55]	CPU_I2C_SDA_TS	<<<
[55]	CPU_I2C_SCL_TS	<<<
[65]	CPU_I2C_SDA_TP	<<<
[65]	CPU_I2C_SCL_TP	<<<
[56]	P_DET#	<<<
[69,70]	CPU_I2C_SDA_SENSOR#	<<<
[69,70]	CPU_I2C_SCL_SENSOR#	<<<
[62]	CPU_I2C_SDA_GNSS	<<<
[62]	CPU_I2C_SCL_GNSS	<<<
[69]	GSEN_INT1	<<<
[70]	LNG2DMTR_INT1	<<<
[24]	NB_MODE#	<<<
[24]	LID_CL#_NB_R	>>>
[24]	LID_CL#_TAB_R	>>>
[56]	P_CLK	<<<
[56]	P_DATA	<<<
[91]	TPM_PIRQ#	<<<
[40]	PCH_TOUCH_SCREEN_EN	<<<
[55]	LCD_CBL_DET#	>>>
[21,61]	CNV_BRI_RSP	<<<
[21,61]	CNV_RGI_RSP	<<<
[68]	SBIOS_TX	<<<
[56]	IR_CAM_DET#	>>>
[56]	ISH_P_SENSOR_INT#_1P8	>>>
[56]	P_SENSOR_PWR_SAVE#_1P8	<<<
[33]	HOST_SD_WP#	>>>
[29]	SPKR	>>>
[62]	WWAN_FULL_PWR_EN_R	<<<
[61,62]	CNV_MFUART2_TXD	<<<
[61,62]	CNV_MFUART2_RXD	<<<
[24,27]	SPKR	<<<
[56]	ISH_ALS_INT#	>>>
[24]	SML0B_SMLDATA	<<<
[24]	SML0B_SMLCLK	<<<
[24]	ISH_TABLE_MODE#	<<<



Do Not Stuff
Do Not Stuff

Do Not Stuff
Do Not Stuff

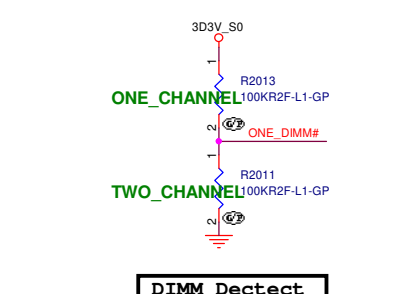
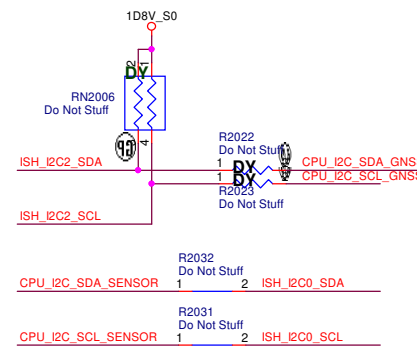
Do Not Stuff



ONE_DIMM#	DC53
NRB_BIT	DA51
HOST_SD_WP#	DC49
SPKR	DC50
SPK_DET#	DC52
LCD_CBL_DET#	CY49
PCH_TOUCH_SCREEN_EN	CY53
SBIOS_TX	DV21
WWAN_FULL_PWR_EN	DT21
P_SENSOR_PWR_SAVE#_1P8	DR21
P_DET#	DW21
1PCH_SSD_PWR_EN	DV19
12.7MM_CAM_DET#	DT19
IR_CAM_DET#	DR19
TPM_PIRQ#	DU19
CPU_UART2_TXD	DJ21
CPU_UART2_RXD	DJ23
CPU_I2C_SDA	DF21
CPU_I2C_SCL	DF23
ISH_P_SENSOR_INT#_1P8	DJ29
ISH_P_SENSOR_INT#_1P8	DJ31
1SPK_DET1#	DF29
CNV_MFUART2_TXD	DF25
CNV_MFUART2_RXD	DF27

CPU1F	6 OF 21
GPP_B16/GSPI0_CLK	GPP_B16/GSPI0_CLK
GPP_B18/GSPI0_MOSI	GPP_B18/GSPI0_MOSI
GPP_B17/GSPI0_MISO	GPP_B17/GSPI0_MISO
GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#	GPP_B14/SPKR/TIME_SYNC1/GSPI0_CS1#
GPP_B15/GSPI0_CS0#	GPP_B15/GSPI0_CS0#
GPP_B20/GSPI1_CLK	GPP_B20/GSPI1_CLK
GPP_B22/GSPI1_MOSI	GPP_B22/GSPI1_MOSI
GPP_B21/GSPI1_MISO	GPP_B21/GSPI1_MISO
GPP_B19/GSPI1_CS0#	GPP_B19/GSPI1_CS0#
GPP_C9/UART0_TXD	GPP_C9/UART0_TXD
GPP_C8/UART0_RXD	GPP_C8/UART0_RXD
GPP_C11/UART0_CTS#	GPP_C11/UART0_CTS#
GPP_C10/UART0_RTS#	GPP_C10/UART0_RTS#
GPP_C13/UART1_TXD	GPP_C13/UART1_TXD
GPP_C12/UART1_RXD	GPP_C12/UART1_RXD
GPP_C15/UART1_CTS#	GPP_C15/UART1_CTS#
GPP_C14/UART1_RTS#	GPP_C14/UART1_RTS#
GPP_C21/UART2_TXD	GPP_C21/UART2_TXD
GPP_C20/UART2_RXD	GPP_C20/UART2_RXD
GPP_C23/UART2_CTS#	GPP_C23/UART2_CTS#
GPP_C22/UART2_RTS#	GPP_C22/UART2_RTS#
GPP_C17/I2C0_SCL	GPP_C17/I2C0_SCL
GPP_C16/I2C0_SDA	GPP_C16/I2C0_SDA
GPP_C19/I2C1_SCL	GPP_C19/I2C1_SCL
GPP_C18/I2C1_SDA	GPP_C18/I2C1_SDA
GPP_H5/I2C2_SCL	GPP_H5/I2C2_SCL
GPP_H4/I2C2_SDA	GPP_H4/I2C2_SDA
GPP_H7/I2C3_SCL	GPP_H7/I2C3_SCL
GPP_H6/I2C3_SDA	GPP_H6/I2C3_SDA
GPP_H9/I2C4_SCL/CNV_MFUART2_TXD	GPP_H9/I2C4_SCL/CNV_MFUART2_TXD
GPP_H8/I2C4_SDA/CNV_MFUART2_RXD	GPP_H8/I2C4_SDA/CNV_MFUART2_RXD

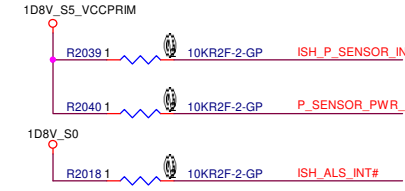
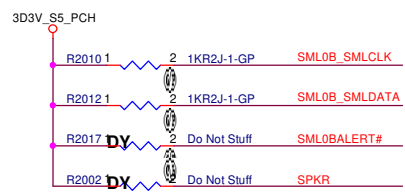
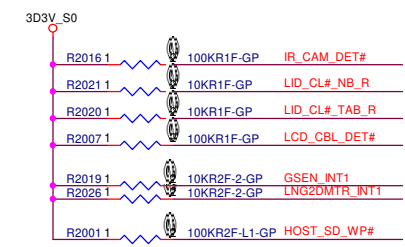
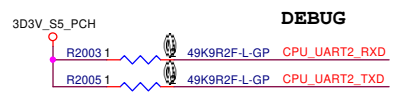
Do Not Stuff



DIMM Detect	
HIGH	1 DIMM
LOW	2 DIMM

GPP_D14/ISH_UART0_TXD	GPP_D14/ISH_UART0_TXD
GPP_D13/ISH_UART0_RXD	GPP_D13/ISH_UART0_RXD
GPP_D16/ISH_UART0_CTS#	GPP_D16/ISH_UART0_CTS#
GPP_D15/ISH_UART0_RTS#	GPP_D15/ISH_UART0_RTS#
GPP_B6/ISH_I2C0_SCL	GPP_B6/ISH_I2C0_SCL
GPP_B5/ISH_I2C0_SDA	GPP_B5/ISH_I2C0_SDA
GPP_B8/ISH_I2C1_SCL	GPP_B8/ISH_I2C1_SCL
GPP_B7/ISH_I2C1_SDA	GPP_B7/ISH_I2C1_SDA
GPP_B10/I2C5_SCL/ISH_I2C2_SCL	GPP_B10/I2C5_SCL/ISH_I2C2_SCL
GPP_B9/I2C5_SDA/ISH_I2C2_SDA	GPP_B9/I2C5_SDA/ISH_I2C2_SDA
GPP_E16/ISH_GP7	GPP_E16/ISH_GP7
GPP_E15/ISH_GP6	GPP_E15/ISH_GP6
GPP_D18/ISH_GP5	GPP_D18/ISH_GP5
GPP_D17/ISH_GP4	GPP_D17/ISH_GP4
GPP_D3/ISH_GP3/BK3/SBK3	GPP_D3/ISH_GP3/BK3/SBK3
GPP_D2/ISH_GP2/BK2/SBK2	GPP_D2/ISH_GP2/BK2/SBK2
GPP_D1/ISH_GP1/BK1/SBK1	GPP_D1/ISH_GP1/BK1/SBK1
GPP_D0/ISH_GP0/BK0/SBK0	GPP_D0/ISH_GP0/BK0/SBK0
GPP_RCAMP	GPP_RCAMP
GPP_T3/I2C7_SCL	GPP_T3/I2C7_SCL
GPP_T2/I2C7_SDA	GPP_T2/I2C7_SDA
GPP_U5/GSPI3_CLK	GPP_U5/GSPI3_CLK
GPP_U4/GSPI3_CS0#	GPP_U4/GSPI3_CS0#

DR27	SML0B_SMLCLK	EC
DW27	SML0B_SMLDATA	
DV25	SML0BALERT#	
DB45	ISH_I2C0_SCL	SENSOR BD, 3.3V
DB44	ISH_I2C0_SDA	
CY39	ISH_I2C1_SCL	ALS Camera, 1.8V
DB47	ISH_I2C1_SDA	
DD47	ISH_I2C2_SCL	WWAN
DD44	ISH_I2C2_SDA	
DJ8	ISH_P_SENSOR_INT#_1P8	
DR7	ISH_LID_CLF#_TAB_R2058_1	2 Do Not Stuff LID_CL#_TAB_R
DR24	ISH_LID_CLF#_NB_R2057_1	2 Do Not Stuff LID_CL#_NB_R
DU25	ISH_NB_MODE	
DV31	ISH_ALS_INT#	
DU31	ISH_TABLE_MODE#	
DT27	ISH_ACC2_INT#	2 Do Not Stuff LNG2DMTR_INT1
DV27	ISH_ACC1_INT#	2 Do Not Stuff GSEN_INT1
DR51	GPP_RCAMP	R2059 1 2 200R2F-L-GP
DN33	GPP_T3/I2C7_SCL	
DT35	GPP_T2/I2C7_SDA	
DG17	GPP_U5/GSPI3_CLK	
DG19	GPP_U4/GSPI3_CS0#	



MULTI BOM

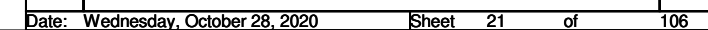
DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU (UART/I2C/ISH)**

Size A3 Document Number **SouthPeak13 TGL** Rev **A00**

Date: Wednesday, October 28, 2020 Sheet 20 of 106

<https://vinafix.com/>

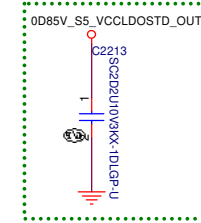


[50]	VCCAUX_SENSE	<<————
[50]	VSSAUX_SENSE	<<————
[50]	CORE_VID0	<<————
[50]	CORE_VID1	<<————
[40]	VNN_CTRL	<<————
[40]	V1P05_CTRL	>>>————
[3,24]	PROCHOT#_CPU	>>>————
[3,44,46,72,74]	PROCHOT#_PD_R	>>>————

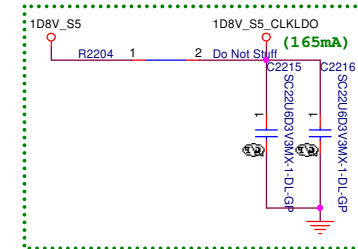


<https://vinafix.com/>

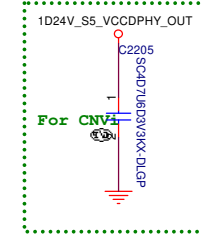
Place cap within
3mm from SOC edge



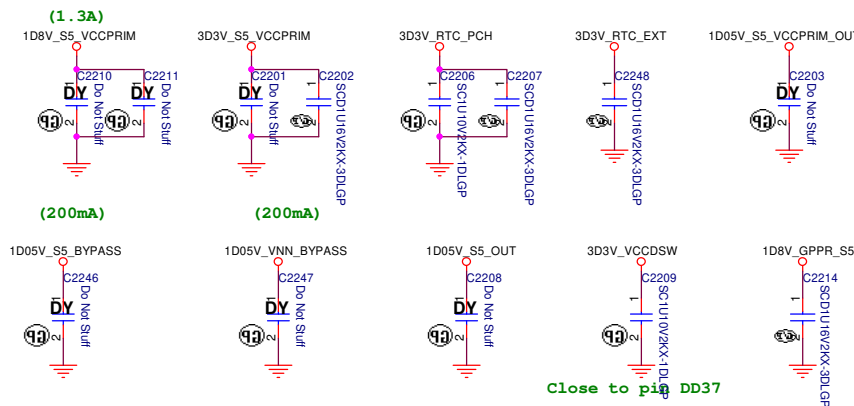
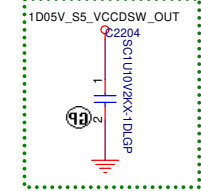
Must take care
this power layout
and add shield GND.



Place cap within
3mm from SOC edge



Trace width > 40mil



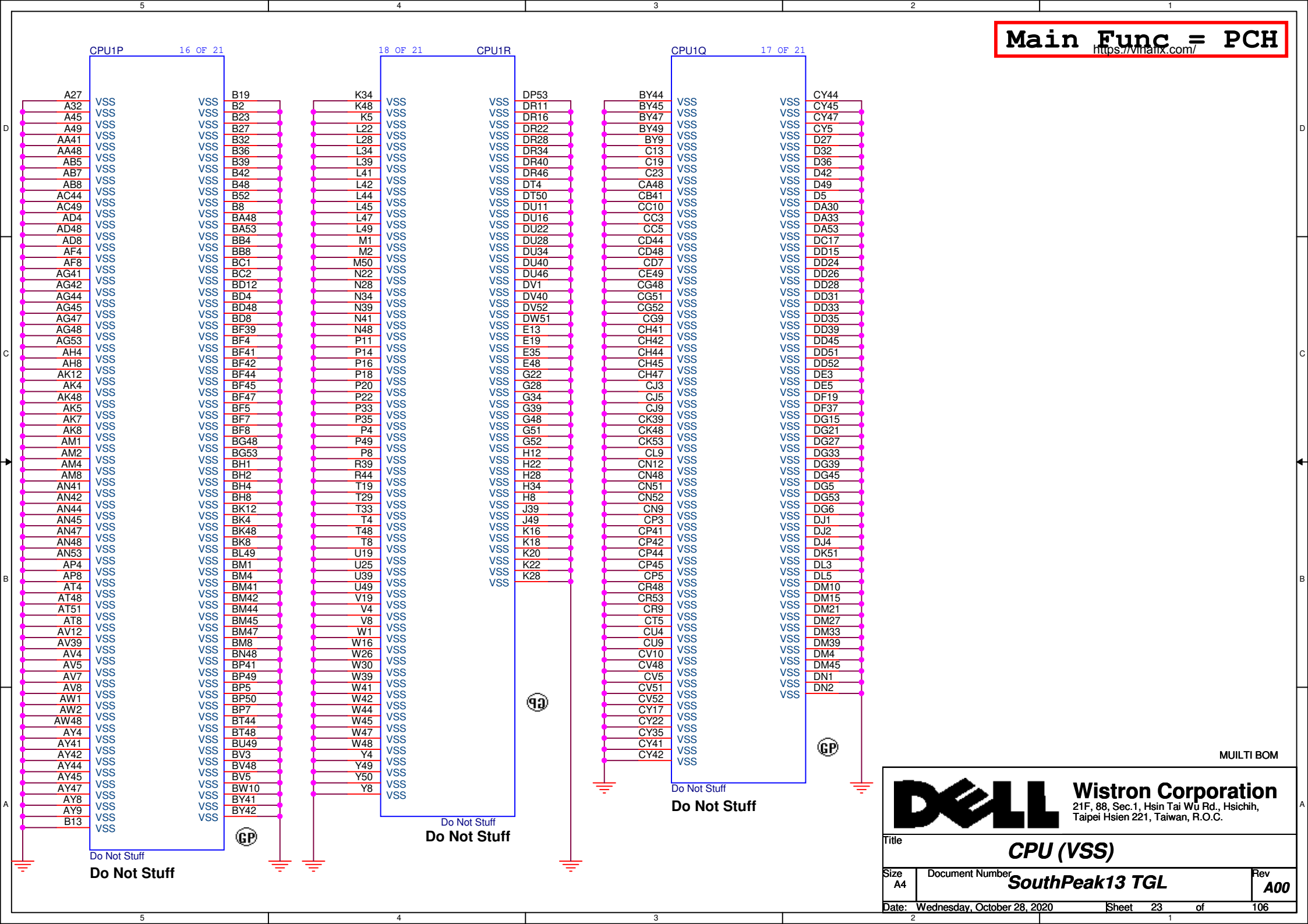
MULTI BOM



Title	CPU (PCH-LP PWR&Caps)
-------	----------------------------------

Size A3	Document Number SouthPeak13 TGL	Rev A00
------------	---	------------

Date: Wednesday, October 28, 2020 Sheet 22 of 106



MULTI BOM

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CPU (VSS)**

Size A4	Document Number SouthPeak13 TGL	Rev A00
---------	--	----------------

Date: Wednesday, October 28, 2020 Sheet 23 of 106

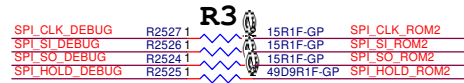


Main Func = BIOS ROM/RTC

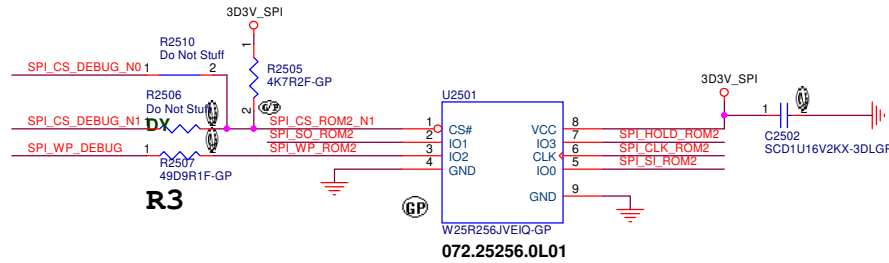
SYSTEM SPI ROM

<https://vinafix.com/>

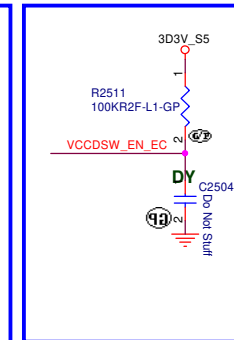
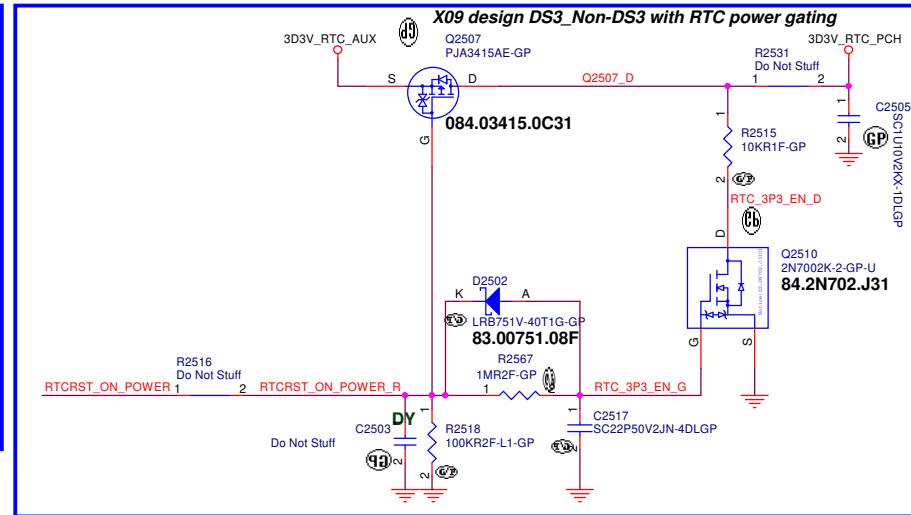
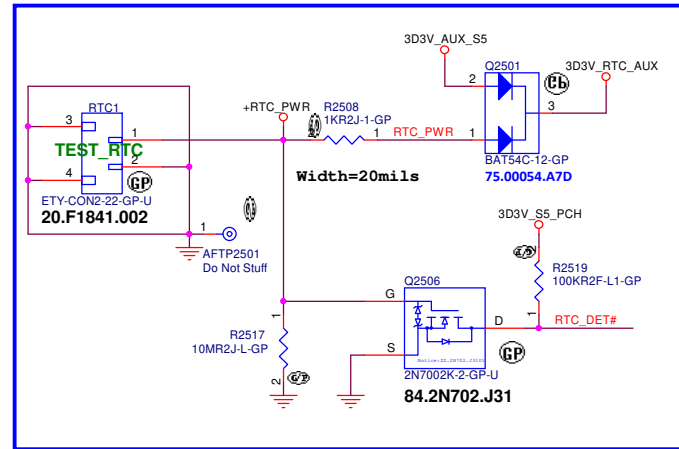
[24,68,91] SPI_CLK_DEBUG >>>
 [24,68,91] SPI_SI_DEBUG >>>
 [24,68,91] SPI_SO_DEBUG >>>
 [24,68] SPI_WP_DEBUG >>>
 [24,68] SPI_HOLD_DEBUG >>>
 [24,68] SPI_CS_DEBUG_N0 >>>
 [24,68] SPI_CS_DEBUG_N1 >>>
 [18,24] RTCRST_ON >>>
 [24] VCCDSW_EN_EC >>>
 [24] RTCRST_ON_POWER >>>
 [18] RTC_DET# <<<



32M ROM(RPMC) :072.25256.0L01 / W25R256JVEIQ



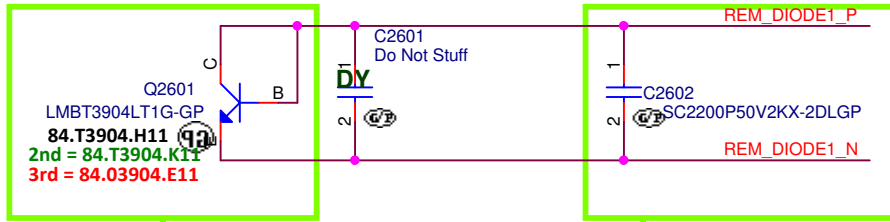
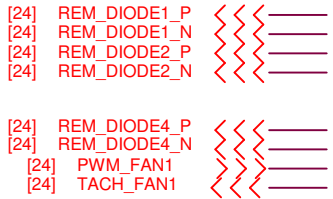
Vendor	Vendor P/N	WISTRON P/N	ROSA M P/N
Winbond	W25R256JVEIQ	072.25256.0L01	072.25256.M006
MXIC	MX77L25650FZ4I42	072.77256.0003	072.77256.M002
GigaDev	GD25R256DYIGR	072.25256.0H03	072.25256.M007
XMC	XM25RH256CXIQT10Q	072.25256.0A41	072.77256.M003



MULTI BOM

Main Func = Thermal / FAN

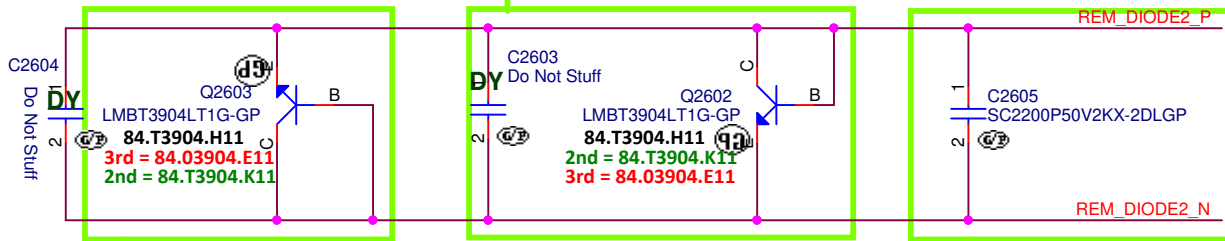
5107 Channel	Location
DP1/DN1	CPU (Q2601)
DP2/DN2	WWAN (Q2602)
DN2a/DP2a	DDR (Q2603)
DP4/DN4	V.R (Q2605)



Layout Note: Place to CPU

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

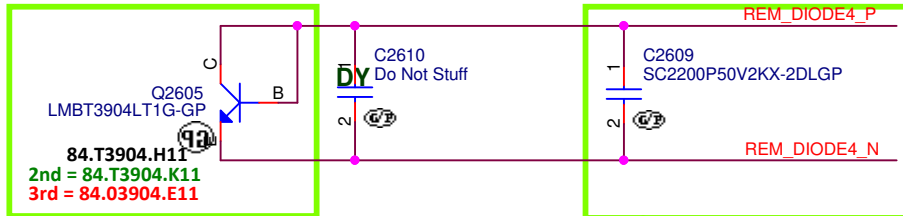
Layout Note: Close to EC



Layout Note:Place to DIMM

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

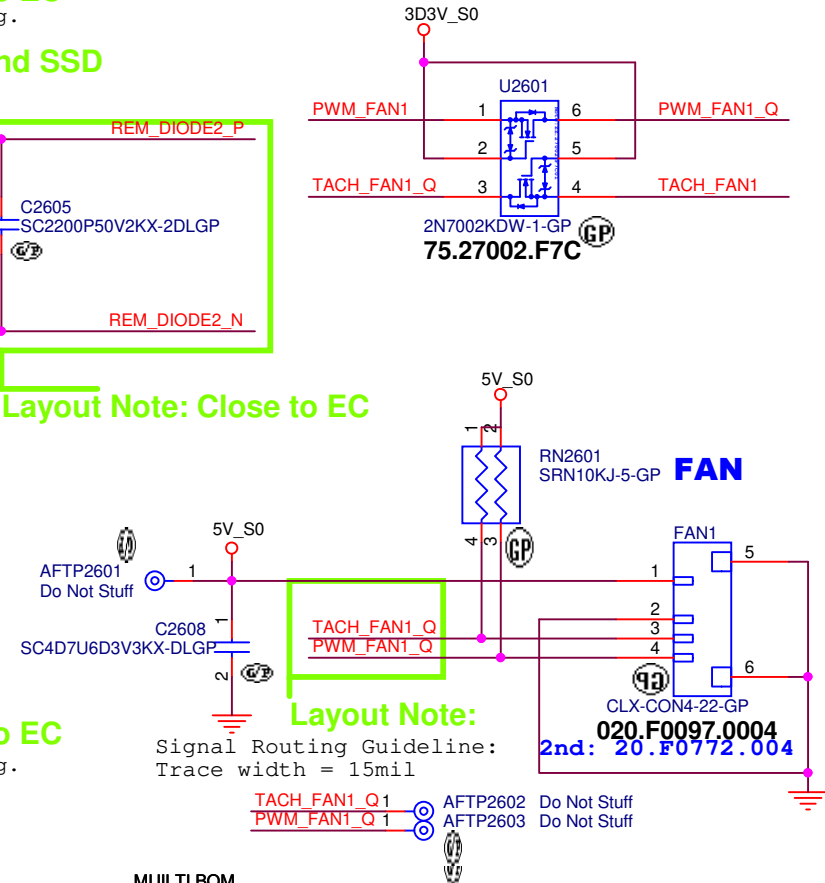
Layout Note: Close to EC



Layout Note:Place to V.R

Both DXN and DXP routing 10 mil trace width and 10 mil spacing.

Layout Note: Close to EC



MULTI BOM



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	INT IO (Thermal/Fan)
-------	-----------------------------

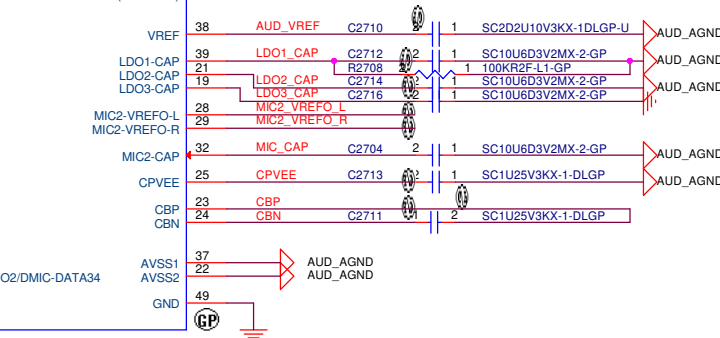
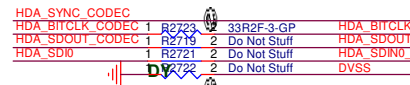
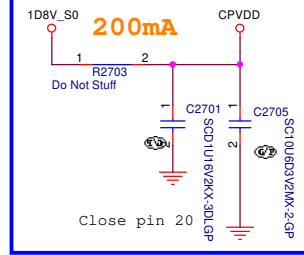
Size A4	Document Number SouthPeak13 TGL
------------	---

Rev
400

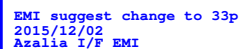
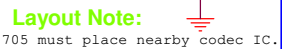
Date: Wednesday, October 28, 2020

Sheet	26	of	106
-------	----	----	-----

[29]	AUD_SPK_L+	>>>	_____
[29]	AUD_SPK_L-	>>>	_____
[29]	AUD_SPK_R-	>>>	_____
[29]	AUD_SPK_R+	>>>	_____
[29]	AUD_HPJD_N	>>>	_____
[24]	NB_MUTE#	>>>	_____
[56]	DMIC_SDA_CODECD	<<<	_____
[56]	DMIC_SCL_CODECD	<<<	_____
[17,24,40,68]	SIO_SLP_S3#	>>>	_____
[20,24]	SPKR	>>>	_____
[24]	BEEP	>>>	_____
[29]	AUD_RING	>>>	_____
[29]	AUD_SELEEVE	>>>	_____
[29]	LINE1_R	>>>	_____
[29]	LINE1_L	>>>	_____
[29]	MIC2_VREF0_R	<<<	_____
[29]	MIC2_VREF0_L	<<<	_____
[29]	AUD_HPOUT_L	<<<	_____
[29]	AUD_HPOUT_R	<<<	_____
[19]	HDA_RST#	>>>	_____
[19]	HDA_SDIO	>>>	_____
[19]	HDA_SDOUT_CODECD	>>>	_____
[19]	HDA_SYNC_CODECD	>>>	_____
[19]	HDA_BITCLK_CODECD	>>>	_____



Layout Note:



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title				Audio (Codec ALC3254)			
Size	Document Number					Rev	
A3	SouthPeak13 TGL					A00	
Date:	Wednesday, October 28, 2020			Sheet	27	of	106

5

4

3

2

1

<https://vinafix.com/>

D

D

C

C


B

B

A

A

MULTI BOM

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title Audio (RSVD) (Audio AMP)					
Size A4	Document Number SouthPeak13 TGL				Rev A00
Date: Wednesday, October 28, 2020			Sheet 28 of 106		

Main Func = Audio

Layout Note:

Speaker trace width >40mil @ 2W4ohm speaker power

<https://vinafix.com/>

Speaker

[27] AUD_SPK_L+
[27] AUD_SPK_L-
[27] AUD_SPK_R+
[27] AUD_SPK_R-

[27] MIC2_VREFO_R
[27] MIC2_VREFO_L

[27] AUD_RING

[27] AUD_HPOUT_L

[27] LINE1_L

[27] AUD_HPOUT_R

[27] LINE1_R

[27] AUD_SELEEVE

[27] AUD_HPJD_N

[20] SPK_DET#

AUD_SPK_L+

AUD_SPK_L-

AUD_SPK_R+

AUD_SPK_R-

EL2901 1

EL2902 1

EL2903 1

EL2904 1

HCB1005KF-121T20-GP

HCB1005KF-121T20-GP

HCB1005KF-121T20-GP

HCB1005KF-121T20-GP

main: 68.00358.031
2nd: 068.00006.0041

3D3V_S0

R2915
100KR2F-L1-GP

SPK_DET#

HI	YG
LOW	FG

2017/03/27 modify by EMI suggest

SPK_DET#

ACES-CON6-20-GP-U

20.F1639.006

2nd: 020.F1263.0006

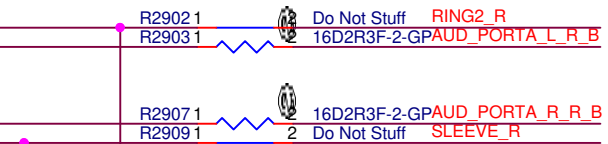
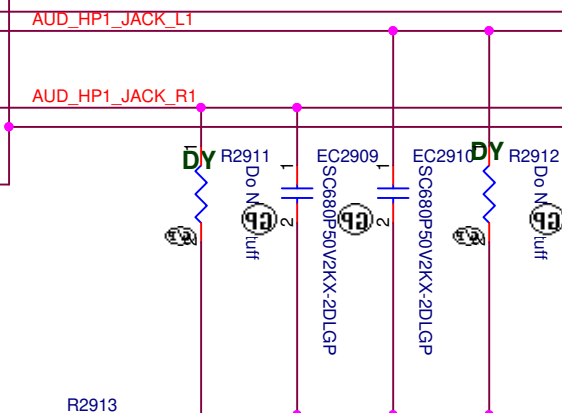
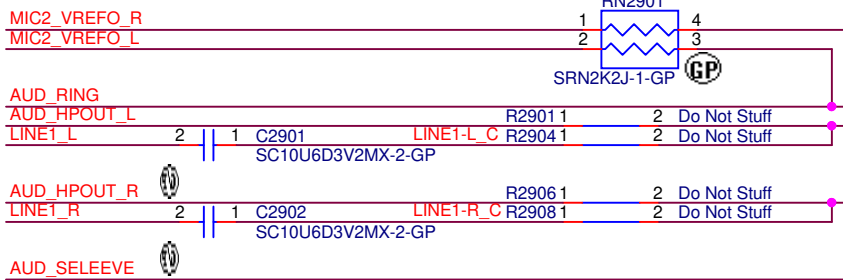
AUD_SPK_L- C	1	AFTP2901
AUD_SPK_L+ C	1	AFTP2902
AUD_SPK_R- C	1	AFTP2903
AUD_SPK_R+ C	1	AFTP2904

CONN	Pin	Net name
Pin1	SPK L+	
Pin2	SPK L-	
Pin3	SPK R-	
Pin4	SPK R+	
Pin5	SPK_DET#	
Pin6	GND	

Layout Note:

R2901 must place nearby AUD1.

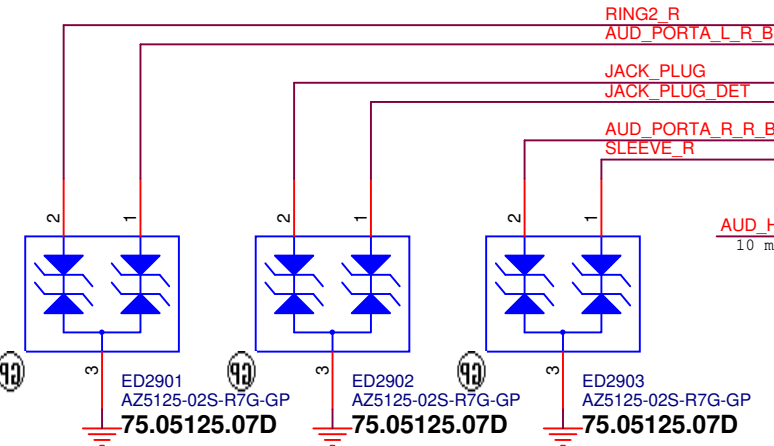
AUD_AGN



Universal Jack

RING2_R	3
AUD_PORTA_L_R_B	1
JACK_PLUG	5
JACK_PLUG_DET	6
AUD_PORTA_R_R_B	2
SLEEVE_R	4
MS	

AUD_AGN
AUDIO-JK724-GP-U
022.10002.M006



AUD_HPJD_N
10 mils
JACK_PLUG
10 mils
JACK_PLUG_DET
10 mils
AUD_AGN

Delay circuit

AUD_AGN
MULTI BOM



Wistron Corporation


21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title Audio (HP/SPK/MIC Jack)


Size A4 Document Number SouthPeak13 TGL Rev A00

Date: Wednesday, October 28, 2020 Sheet 29 of 106

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Audio (HP/SPK/MIC Jack)			
Size A4	Document Number SouthPeak13 TGL		Rev A00
Date: Wednesday, October 28, 2020		Sheet 30	of 106

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Commercial (Intel LAN)

Size

A4

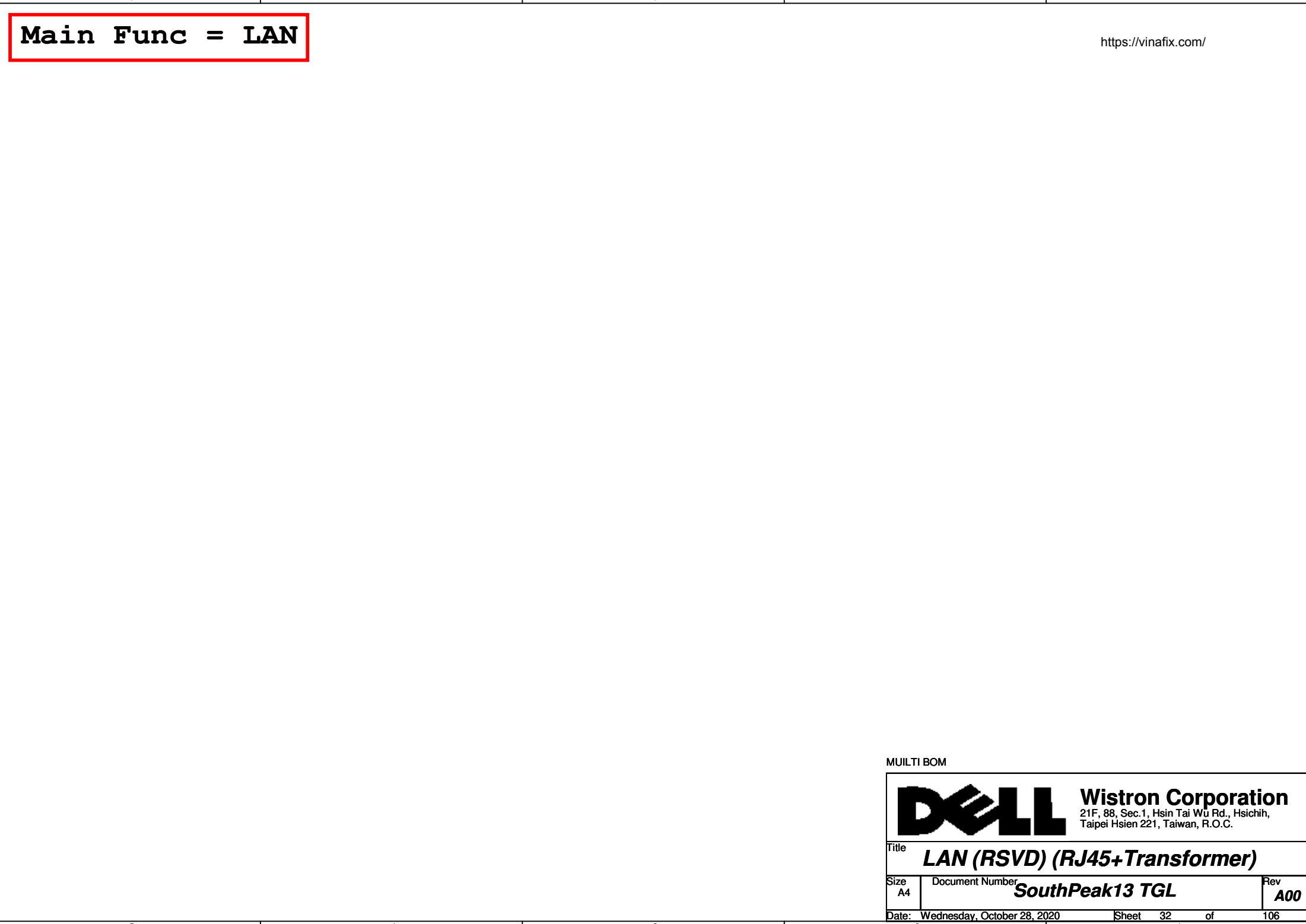
Document Number

Rev


A00

Date: Wednesday, October 28, 2020

Sheet 31 of 106



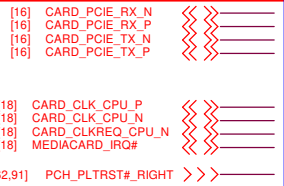
MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title LAN (RSVD) (RJ45+Transformer)		
Size A4	Document Number SouthPeak13 TGL	Rev A00
Date: Wednesday, October 28, 2020		Sheet 32 of 106

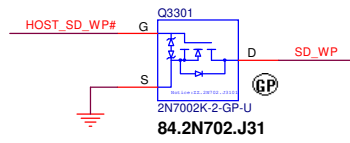
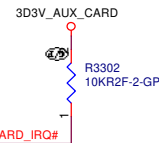
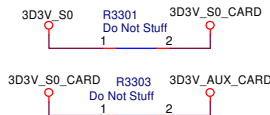
Main Func = Card Reader

3D3V_S0_CARD

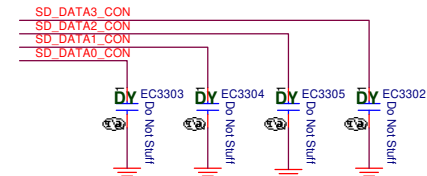
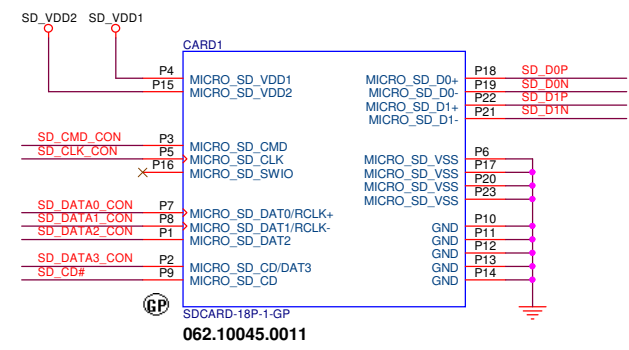
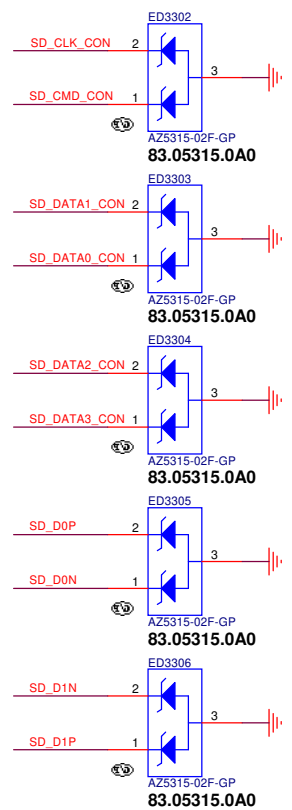
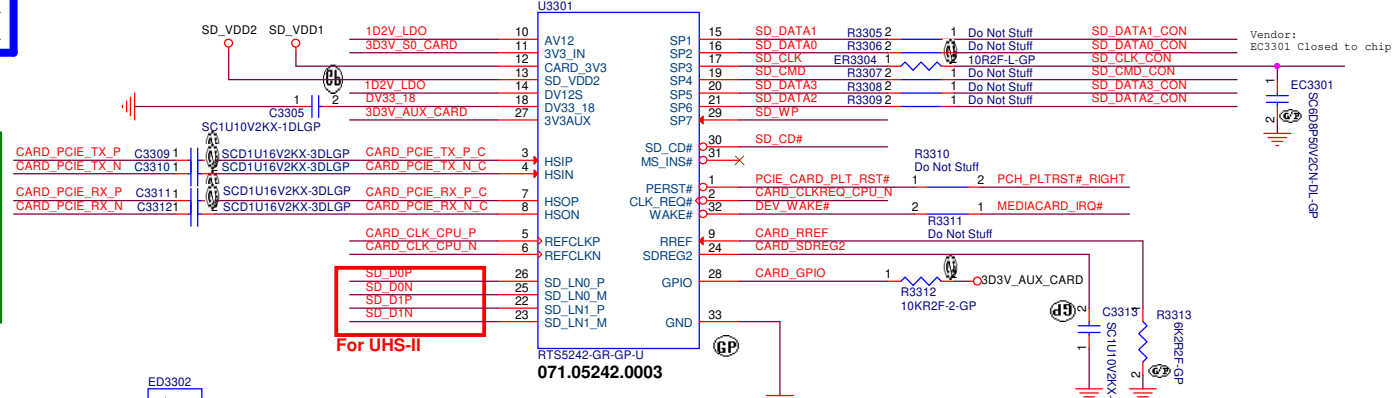
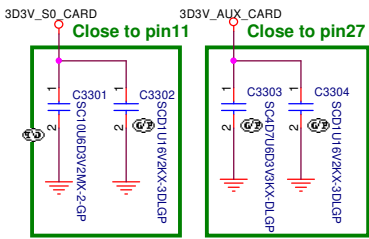
<https://vinafix.com/>



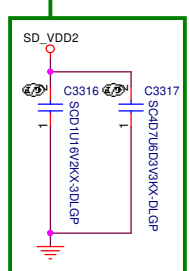
850mA



Layout Note:



Layout Note:Close to Card Reader CONN



MULTI BOM

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **CARDREADER (SDIO/SD Conn)**

Size A3 Document Number **SouthPeak13 TGL** Rev **A00**

Date: Wednesday, October 28, 2020 Sheet 33 of 106

5

4

3

2

1

D

D

C

C


B

B

A

A

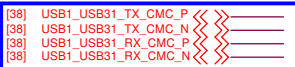
MULTI BOM

 <div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title <div>USB (RSVD) (USB2.0 CONN)</div>		
Size <div>A4</div>	Document Number <div>SouthPeak13 TGL</div>	Rev <div>A00</div>
Date: Wednesday, October 28, 2020		Sheet 34 of 106

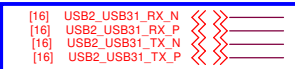
Main Func = USB 3.0 USB3/USB31-1/USB20-4/PowerShare

<https://vinafix.com/>

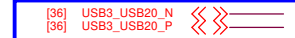
USB3.1 PORT1



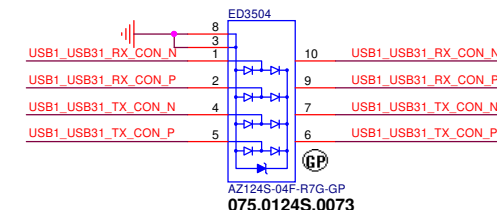
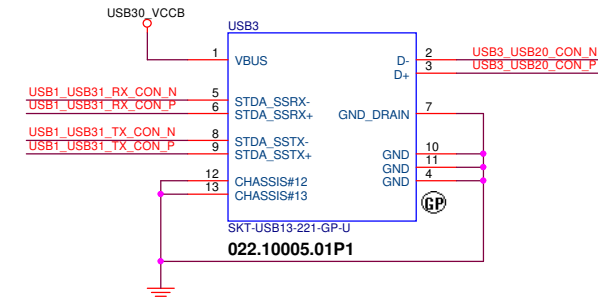
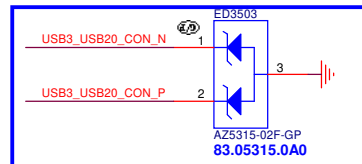
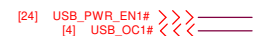
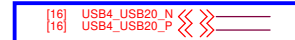
USB3.1 PORT2



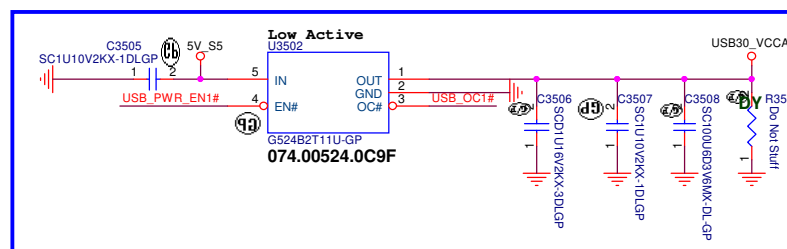
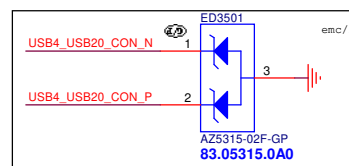
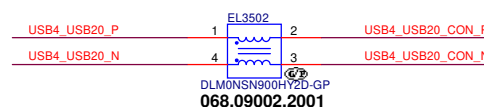
USB2.0 port3



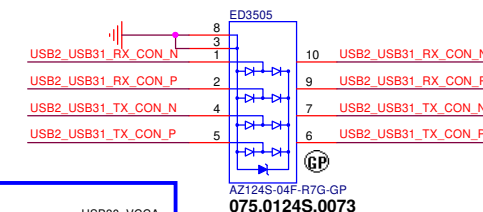
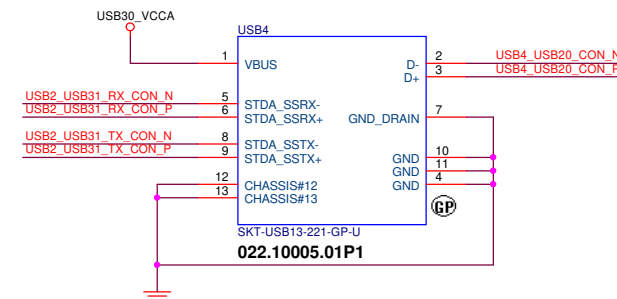
USB2.0 port4



USB4/USB31-2/USB20-5



EXT Port1 Right Side, Support Power Share




MULTI BOM

DELL Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title USB (USB3.0 CONN)	
Size A3	Document Number SouthPeak13 TGL
Date: Wednesday, October 28, 2020	Sheet 35 of 106

<https://vinafix.com/>

106

MULTI BOM

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title USB (RSVD) (PCIE to USB3.0)					
Size A4		Document Number SouthPeak13 TGL			Rev A00
Date: Wednesday, October 28, 2020			Sheet 37 of 106		


<https://vinafix.com/>



Size A4	Document Number SouthPeak13 TGL	Rev A00
------------	---	-------------------

Date: Wednesday, October 28, 2020 Sheet 38 of 106

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Sequence (RSVD)

Size
A4

Document Number
SouthPeak13 TGL

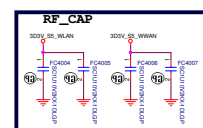
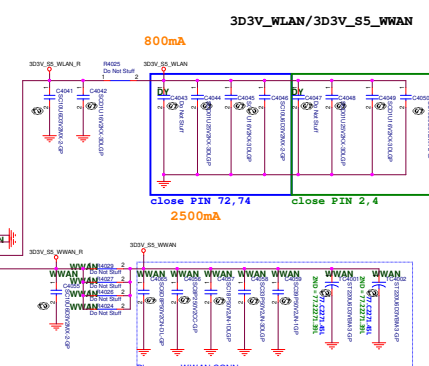
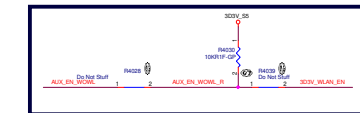
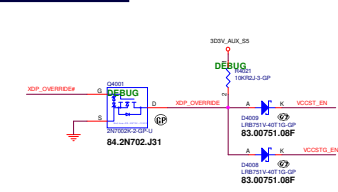
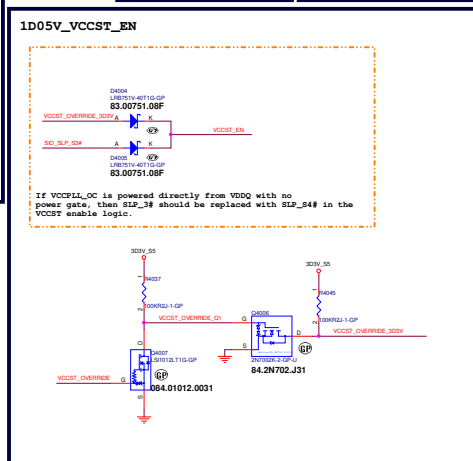
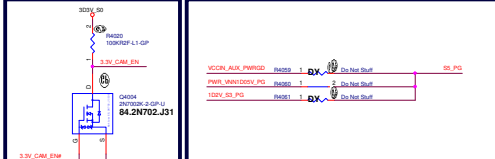
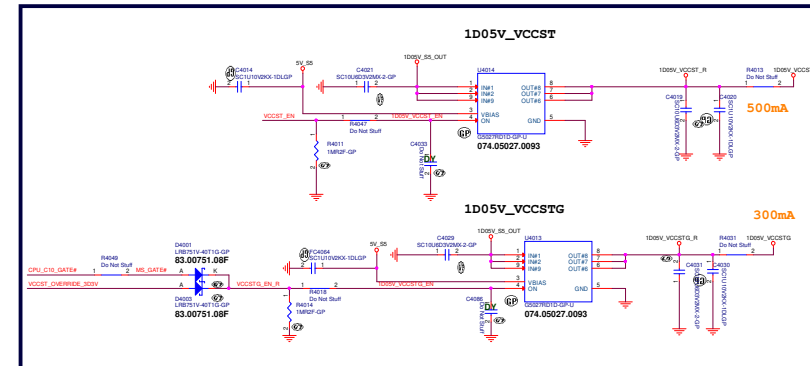
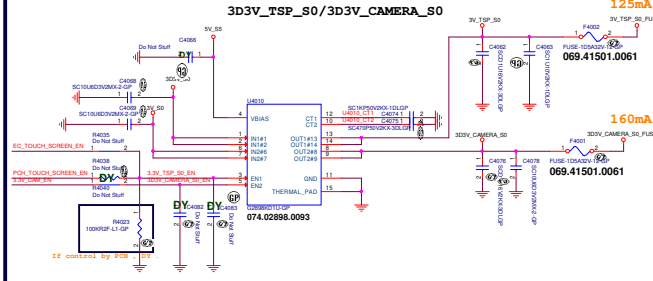
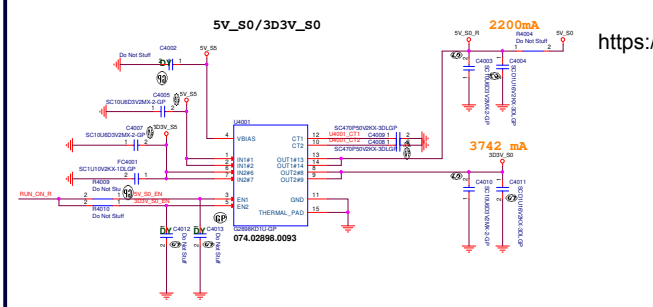
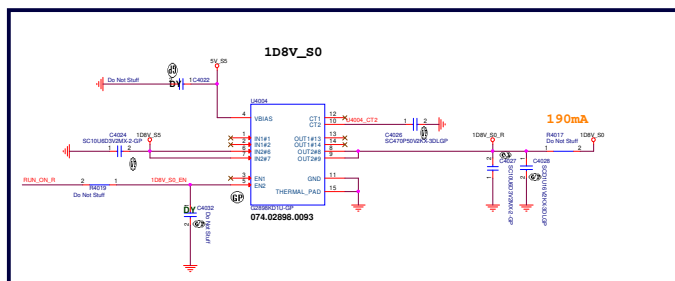
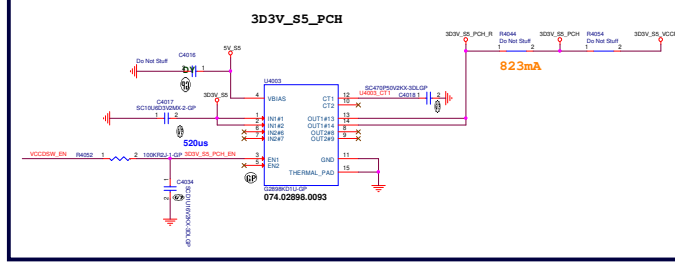
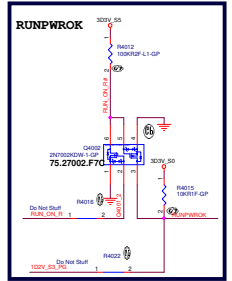
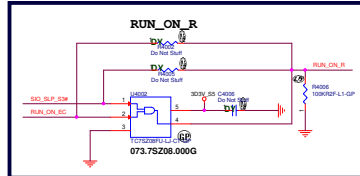
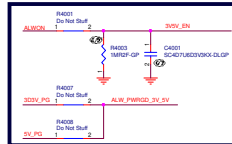
Rev
A00

Date: Wednesday, October 28, 2020Sheet 39 of 106

```

[24.43] ALMON >>>
[24.44] 300V_EN <<<
[24.45] 300V_PG <<<
[24.46] 3V_PG >>>
[24.47] ALL_PIRQD_3V_EN <<<
[24.48] ALLEN_WOVL <<<
[24.49] 3.2V_WOVL_EN <<<
[24.50] NOP_OVERRIDE <<<
[17.91] CPU_C1_GATE# <<<
[24.51] RUN_OA <<<
[24.52] VCCDS_EN <<<
[17.24.53] SCLF_SLP_SUSP <<<
[17.24.54] SCLF_SLP_SCS <<<
[24.55] RUN_OA_EN <<<
[24.56] RUNWAKEP <<<
[24.57] EC_TOUCH_SCREEN_EN <<<
[24.58] EC_TOUCH_SCREEN_EN <<<
[24.59] 3.3V_GAB_EN# <<<
[24.60] VIFPS_CTL <<<
[24.61] 120V_SL3_PG <<<
[24.62] ESP_RESET# <<<
[24.63] VCCIN_AEN_PIRQD <<<
[24.64] PWBL_UNEN <<<
[24.65] PWBL_120V_EN <<<
[24.66] VCCST_OVERRIDE <<<
[24.67] VML_CTL <<<
[24.68] PWBL_UNDERTOP_PG <<<
[24.69] SL_PG >>>

```



5

4

3

2

1

D

D

C

C


B

B

A

A

MULTI BOM



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Sequence (RSVD) (DS3/S0ix)

Size A4	Document Number SouthPeak13 TGL	Rev A00
Date: Wednesday, October 28, 2020	Sheet 41 of	106

5


4

3

2

1

MULTI BOM

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title					
INT IO (RSVD)					
Size	Document Number				Rev
A4	SouthPeak13 TGL				A00
Date: Wednesday, October 28, 2020			Sheet	42	of 106

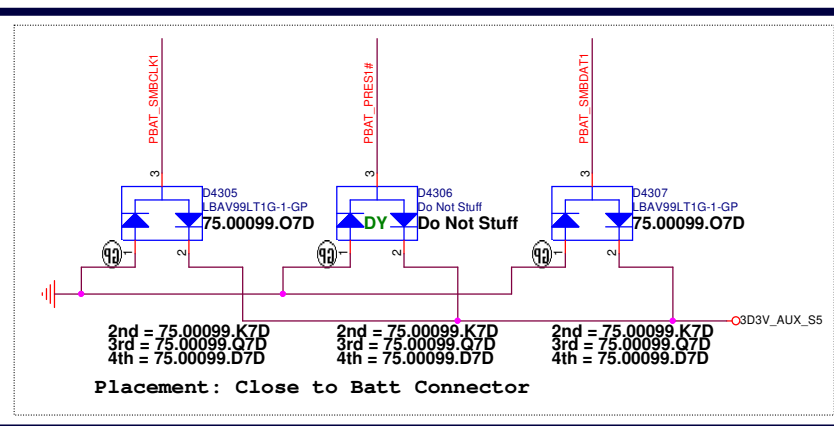
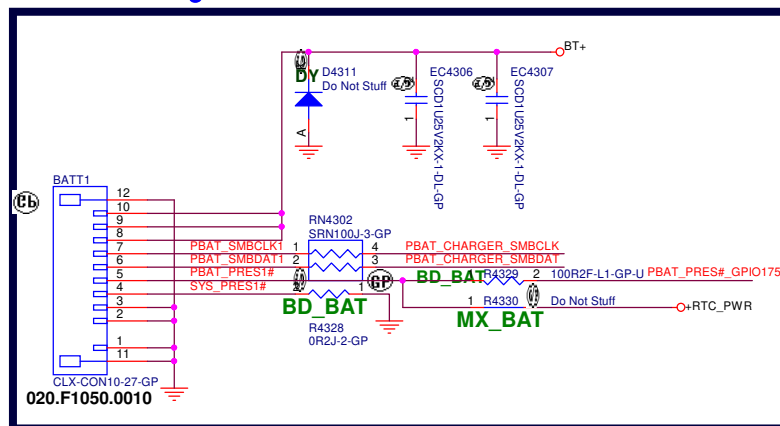
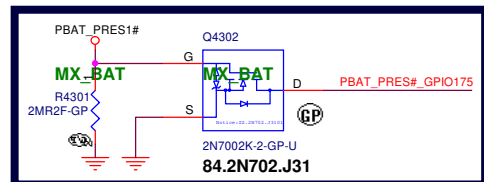
Main Func = DCIN & BATT Com

https://vinafix.com/

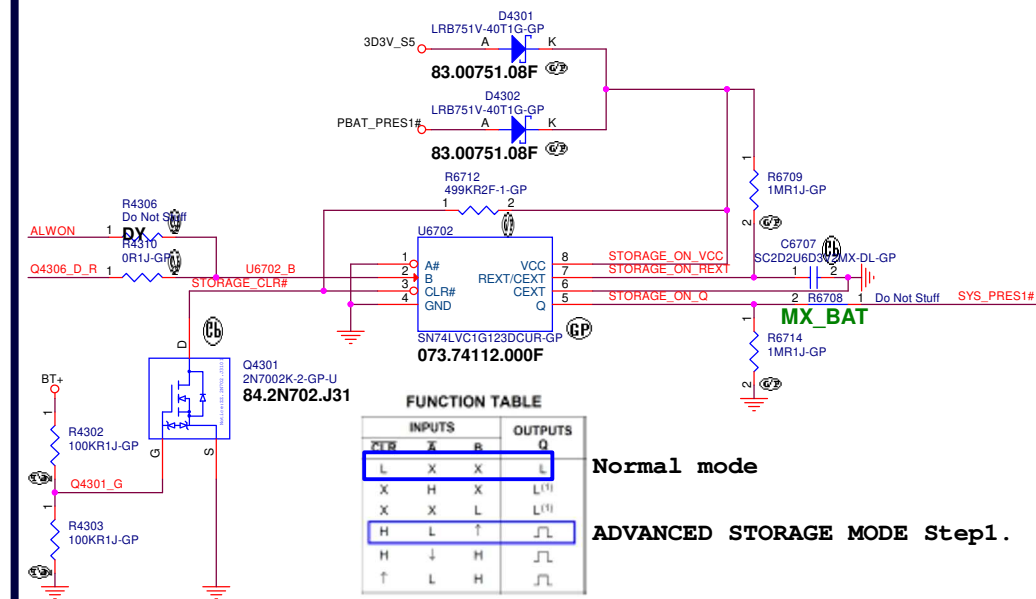
Battery Connector

[24.44] AC_DIS >>>
 [24.74] DCIN1_EN >>>
 [24.44] PBAT_CHARGER_SMBCLK <<<
 [24.44] PBAT_CHARGER_SMBDAT <<<
 [24.44] PBAT_PRES#_GPIO175 <<<
 [24] POWER_SW_IN# <<<

[24.44.74] AC_DISC# <<<
 [24.74] VBUS2_ECOK >>>
 [24.40] ALWON >>>



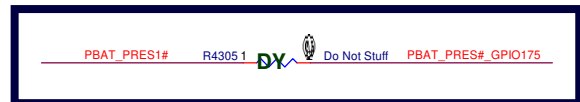
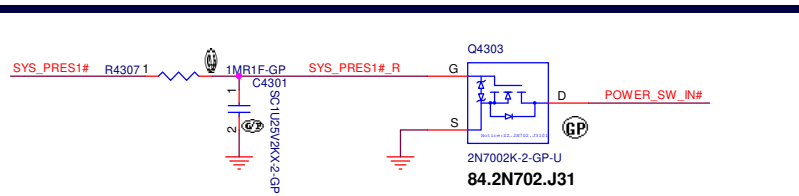
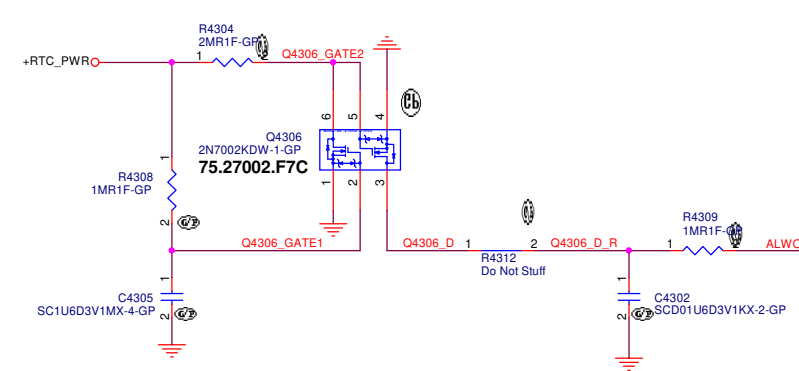
ADVANCED STORAGE MODE



Normal mode

ADVANCED STORAGE MODE Step1.

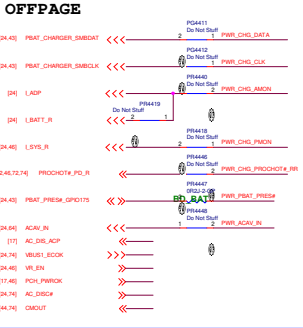
Press power button duration time improvement



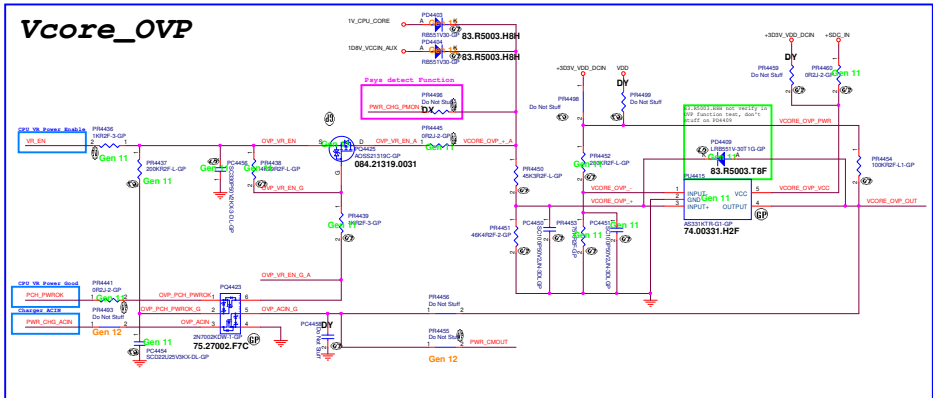
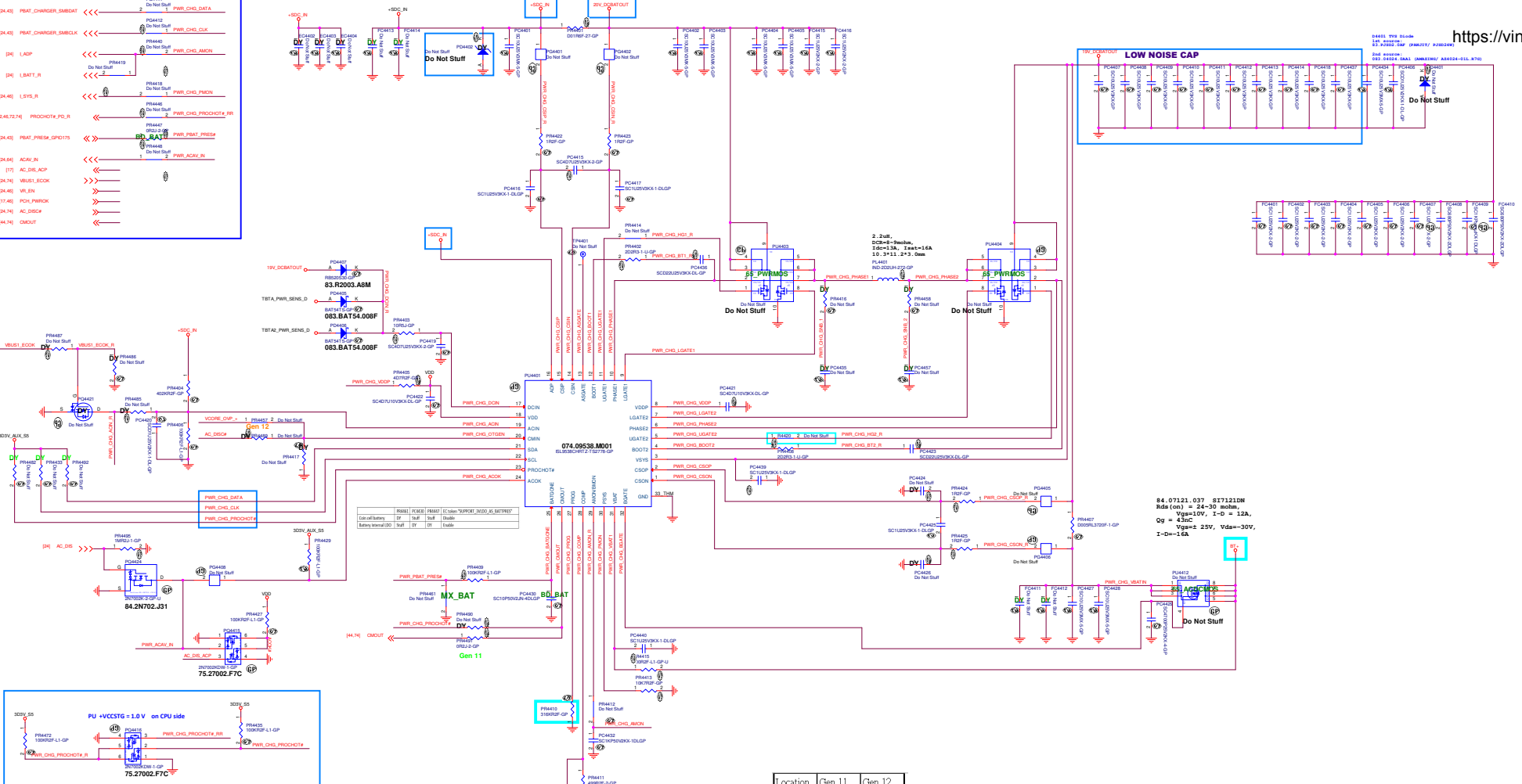
MULTI BOM

DELL Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
 Taipei Hsien 221, Taiwan, R.O.C.

Title: **DC IN/BATT Conn**
 Size: A3 Document Number: Rev: **A00**
 Date: Wednesday, October 28, 2020 Sheet: 43 of 106



Main Func = Power_Charger

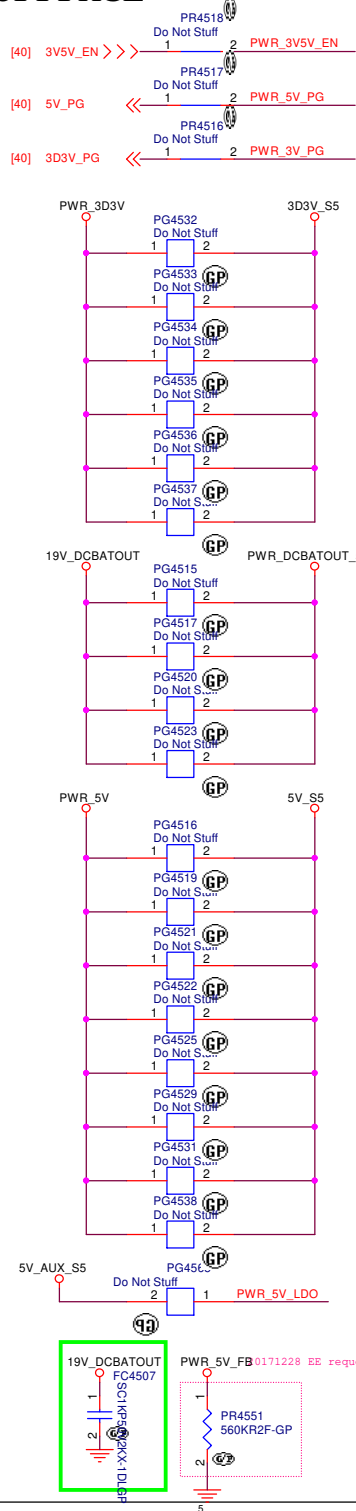


Location	Gen 11	Gen 12
PC4451	Stuff	DY
PC4454	Stuff	DY
PC4456	Stuff	DY
PC4425	Stuff	DY
PR4436	Stuff	DY
PR4437	Stuff	DY
PR4438	Stuff	DY
PR4439	Stuff	DY
PR4441	Stuff	DY
PR4445	Stuff	DY
PR4452	Stuff	DY
PR4453	Stuff	DY
PR4460	Stuff	DY
PR4491	Stuff	DY
PU4415	Stuff	DY
PD4404	DY	Stuff
PR4455	DY	Stuff
PR4457	DY	Stuff

TABLE 22. PROG. FREQ. PROGRAMMING OPTIONS									
MIN	TYP	MAX	CELL #	DEFAULT SWITCHING FREQUENCY	Autonomous charging	DEFAULT AC/DC/PS Frequency			
0	1	7.33MHz	No	0.470					
9.40		7.33MHz	No	0.470					
14.7		1MHz	No	0.470					
20.0		7.33MHz	Yes	0.470					
25.7		7.33MHz	Yes	0.470					
30.0		7.33MHz	Yes	0.470					
35.0		7.33MHz	Yes	0.470					
40.0		7.33MHz	Yes	0.470					
45.0		7.33MHz	Yes	0.470					
50.0		7.33MHz	Yes	0.470					
55.0		7.33MHz	No	0.470					
60.0		7.33MHz	No	0.470					
65.0		7.33MHz	No	0.470					
70.0		7.33MHz	No	0.470					
75.0		7.33MHz	No	0.470					
80.0		7.33MHz	No	0.470					
85.0		7.33MHz	No	0.470					
90.0		7.33MHz	No	0.470					
95.0		7.33MHz	No	0.470					
100		7.33MHz	No	0.470					
105		7.33MHz	No	0.470					
110		7.33MHz	No	0.470					
115		7.33MHz	No	0.470					
120		7.33MHz	No	0.470					
125		7.33MHz	No	0.470					
130		7.33MHz	No	0.470					
135		7.33MHz	No	0.470					
140		7.33MHz	No	0.470					
145		7.33MHz	No	0.470					
150		7.33MHz	No	0.470					
155		7.33MHz	No	0.470					
160		7.33MHz	No	0.470					
165		7.33MHz	No	0.470					
170		7.33MHz	No	0.470					
175		7.33MHz	No	0.470					
180		7.33MHz	No	0.470					
185		7.33MHz	No	0.470					
190		7.33MHz	No	0.470					
195		7.33MHz	No	0.470					
200		7.33MHz	No	0.470					
205		7.33MHz	No	0.470					
210		7.33MHz	No	0.470					
215		7.33MHz	No	0.470					
220		7.33MHz	No	0.470					
225		7.33MHz	No	0.470					
230		7.33MHz	No	0.470					
235		7.33MHz	No	0.470					
240		7.33MHz	No	0.470					
245		7.33MHz	No	0.470					
250		7.33MHz	No	0.470					
255		7.33MHz	No	0.470					
260		7.33MHz	No	0.470					
265		7.33MHz	No	0.470					
270		7.33MHz	No	0.470					
275		7.33MHz	No	0.470					
280		7.33MHz	No	0.470					
285		7.33MHz	No	0.470					
290		7.33MHz	No	0.470					
295		7.33MHz	No	0.470					
300		7.33MHz	No	0.470					

https://vinafix.com/

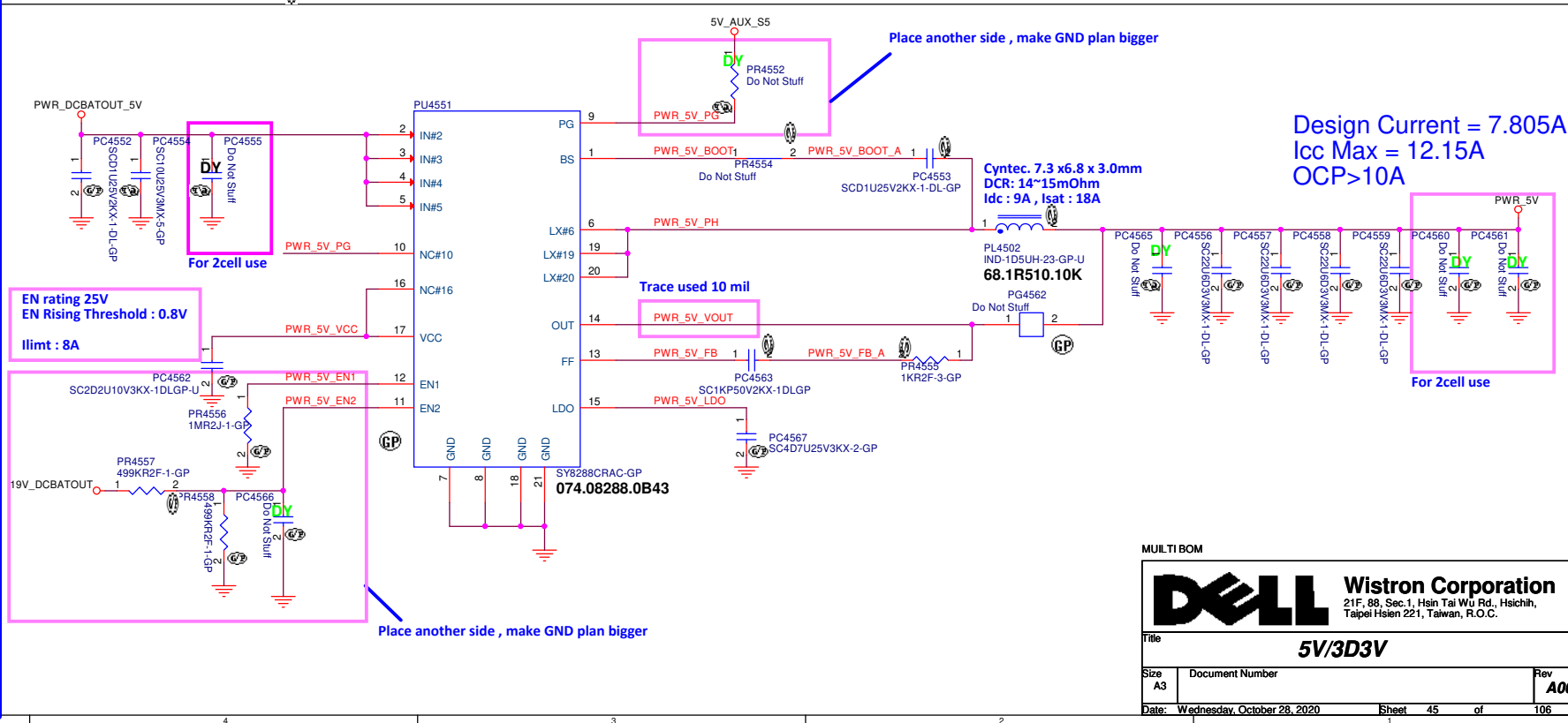
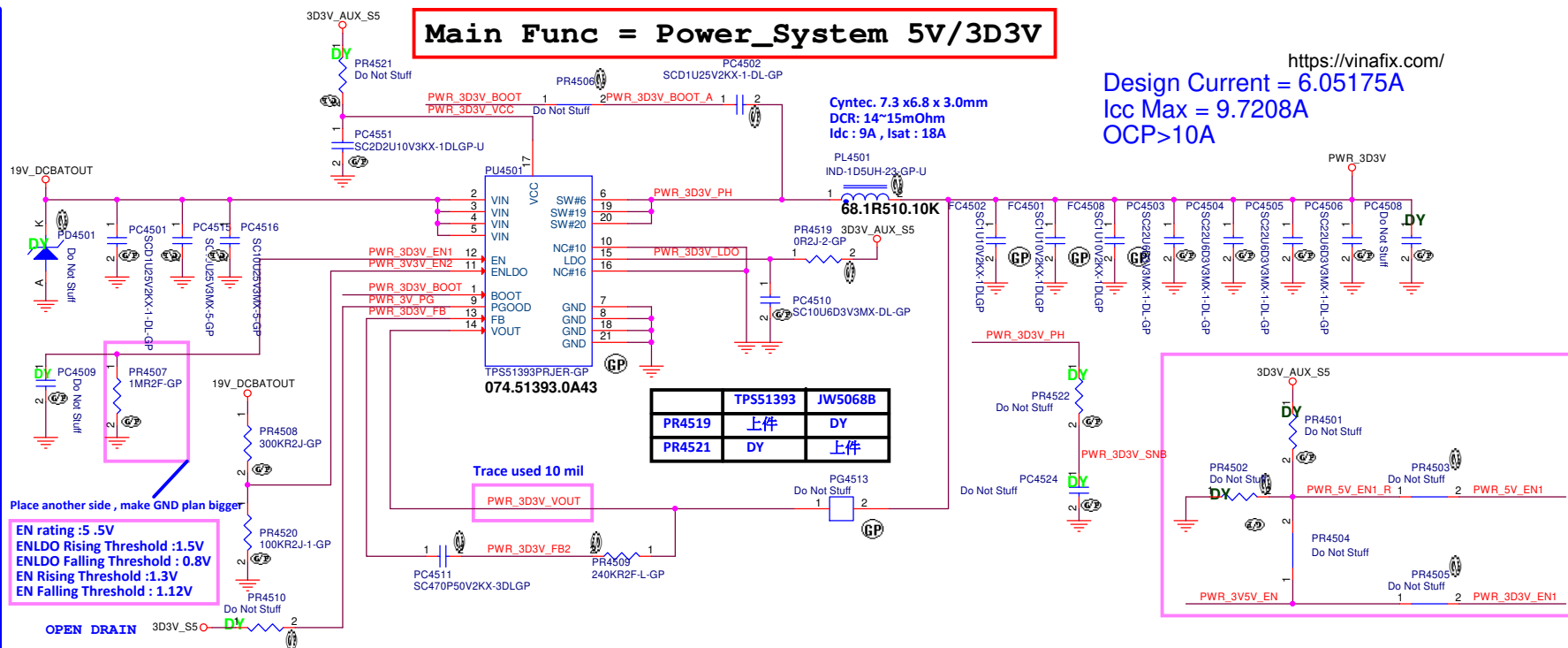
OFFPAGE



Main Func = Power_System 5V/3D3V

<https://vinafix.com/>

Design Current = 6.05175A
Icc Max = 9.7208A
OCP>10A



MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

5V/3D3V

Size
A

Document Number	
-----------------	--

Rev	A00
-----	------------

Date: Wednesday, October 28, 2020

Sheet 45 of 106

[3,22,44,72,74] PROCHOT#_PD_R <<< DY PWR_VCCIN_VRHOT

[7] SVID_CLK_CPU >>> PR4634 Do Not Stuff 1 2 VIDSCK_CPU_R

[7] SVID_DATA_CPU >>> PR4635 Do Not Stuff 1 2 VIDSOUT_CPU_R

[7] SVID_ALERT#_CPU >>> PR4636 Do Not Stuff 1 2 PWR_VCCIN_ALERT#

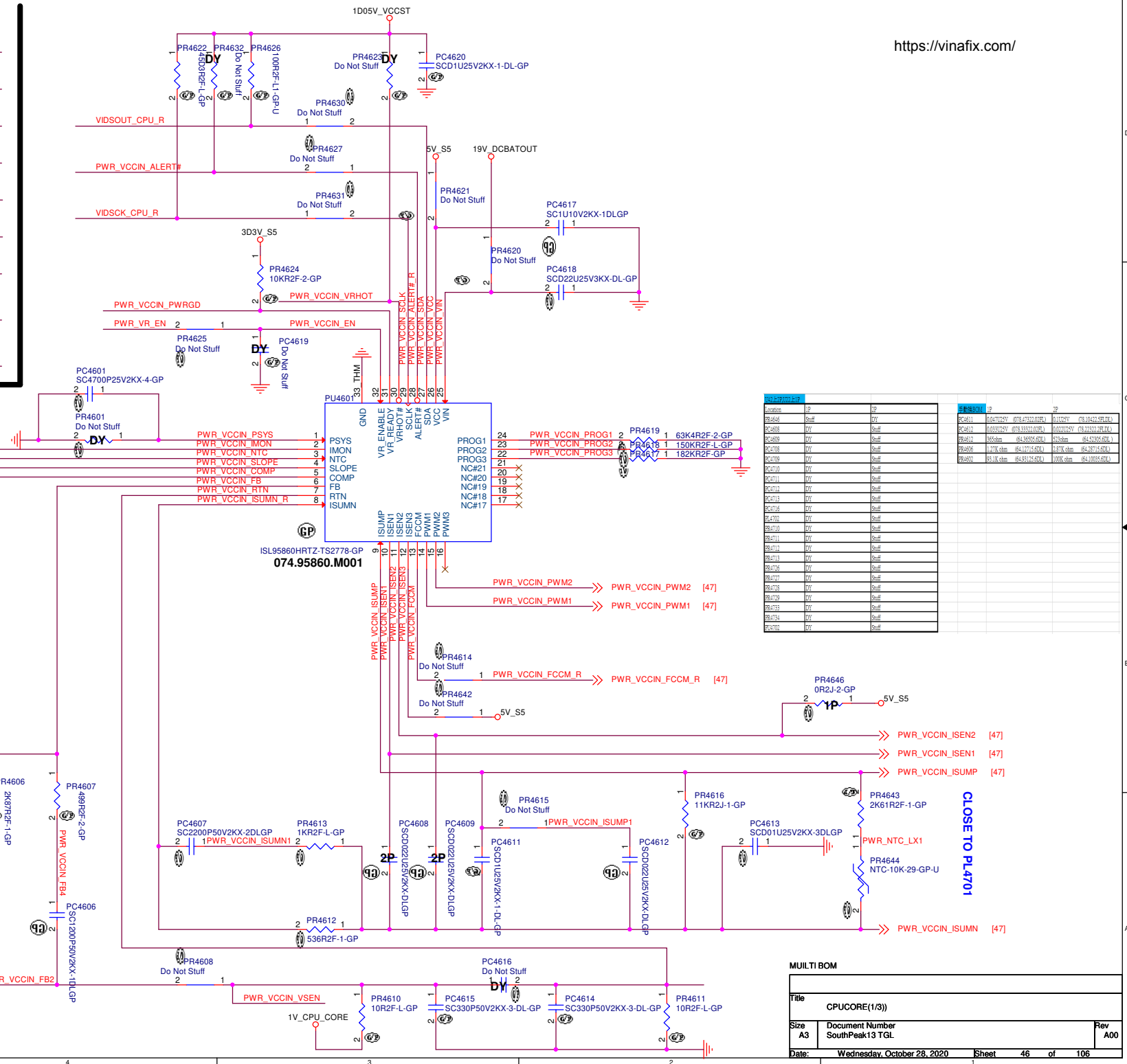
[24,44] VR_EN >>> PR4637 Do Not Stuff 1 2 PWR_VR_EN

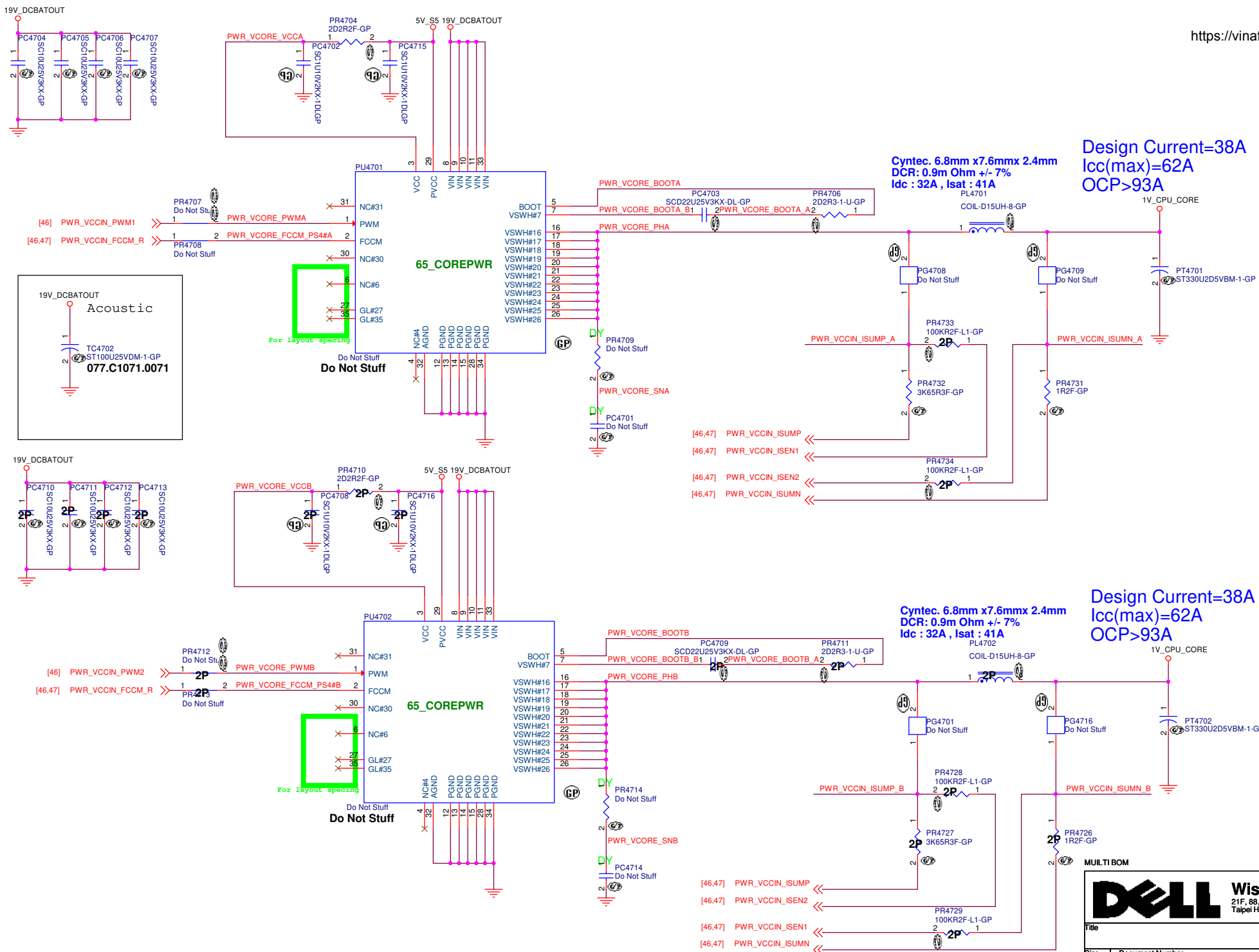
[17,44] PCH_PWROK <<< PR4638 Do Not Stuff 1 2 PWR_VCCIN_PWRGD


[7] VSSCORE_SENSE >>> PR4639 Do Not Stuff 2 1 PWR_VCCIN_RTN

[7] VCCCORE_SENSE >>> PR4640 Do Not Stuff 2 1 PWR_VCCIN_VSEN


[24,44] I_SYS_R >>> PR4641 Do Not Stuff 1 2 PWR_VCCIN_PSYS





MULTI BOM			
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Size A3	Document Number		Rev A00
Date:	Wednesday, October 28, 2020	Sheet 47 of	106

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

POWER

Size

A4

Document Number


Rev

A00

Date: Wednesday, October 28, 2020

Sheet 48 of 106

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title NCP81210MN_CPU_VCCGTUS		
Size A4	Document Number	Rev A00
Date: Wednesday, October 28, 2020		Sheet 49 of 106

OFFPAGE

PH on CPU side

[22] CORE_VID1 >>>
[22] CORE_VID0 >>>

PH on CPU side

[22.50] VCCAUX_SENSE <<<
[22.50] VSSAUX_SENSE <<<

PH on EE Side

[53] PWR_1D8V_PG >>>
[40] VCCIN_AUX_PWRGD <<<

OFFPAGE_GAP

LOGIC

TABLE: MP2941 VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

TABLE: MP2941 FS Selection

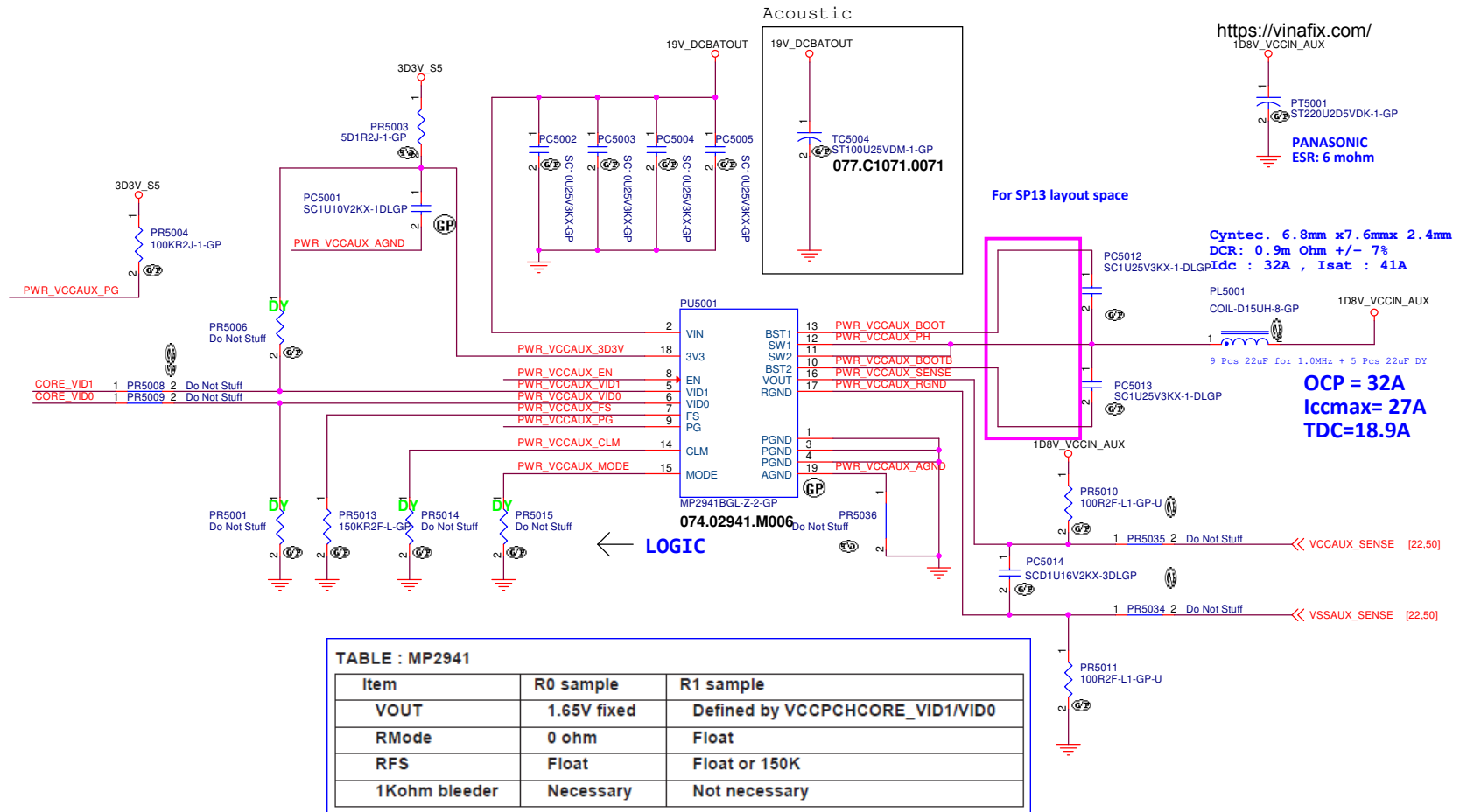
RMode	Fs
0	500kHz
90.9K	700kHz
150K	1000kHz
>230K or float	1200kHz

TABLE: MP2941 CLM/Phase Selection

RCLM	CLM
0	7A
90.9K	10A
150K	13A
>230K or float	16A

TABLE: MP2941 Mode Selection

RMode	Interleaving	VID Down
0	N	Slew down
90.9K	Y	Slew down
150K	Y	Decay
>230K or float	N	Decay



MULTI BOM


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title TPS51486_VDDQ/VTTP/VPP

Size A3 Document Number SouthPeak13 TGL Rev SD

Date: Wednesday, October 28, 2020 Sheet 50 of 106

MULTI BOM



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Size

Custom

Document Number

Rev

A00

Date: Wednesday, October 28, 2020

Sheet 52 of 106

(Reserved)

OFFPAGE

OFFPAGE-GAP

https://vinafix.com/

PH on EE Side

VCCIN_AUX_PWRGD

[40] PWR_VNN_EN >>>
[40] PWR_1D05V_EN >>>

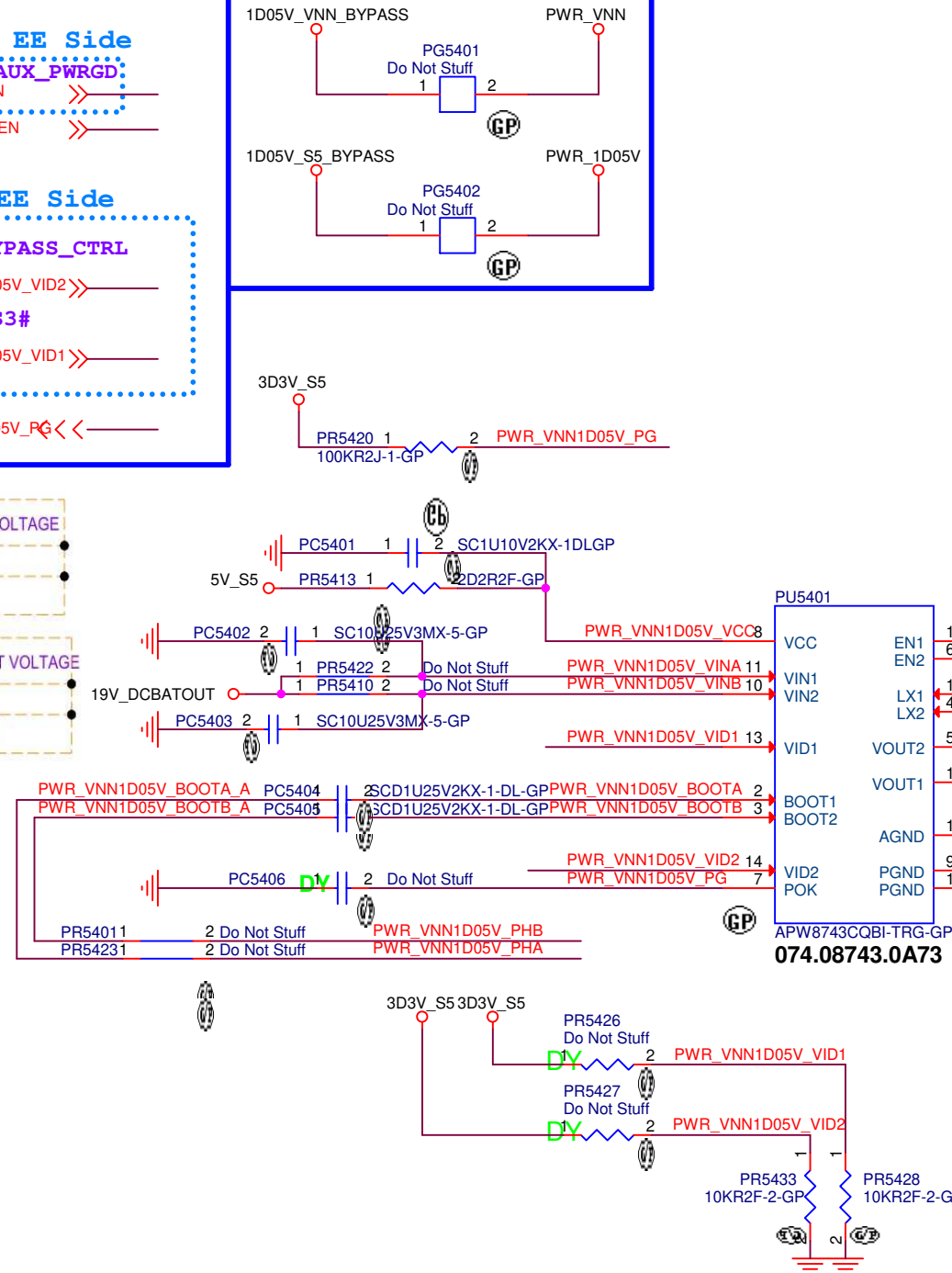
PH on EE Side

1D05V_BYPASS_CTRL

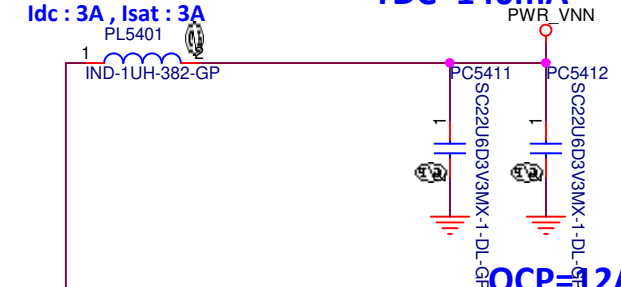
[40] PWR_VNN1D05V_VID2 >>>
PM_SLP_S3#
[40] PWR_VNN1D05V_VID1 >>>
[40] PWR_VNN1D05V_PG <<<

VID1	VNN OUTPUT VOLTAGE
1	0.78 V
0	1.05 V

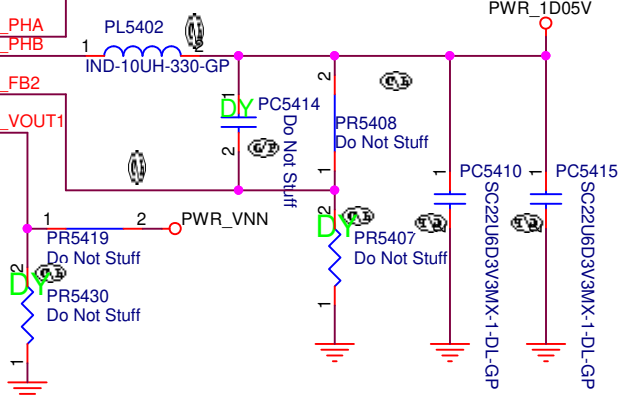
VID2	V1P05 OUTPUT VOLTAGE
1	0.96 V
0	1.05 V



OCP=1A
Iccmax= 200mA
TDC=140mA
Murata. 2.7mm×2.2mmX1.2mm
DCR: 59m Ohm
Idc : 3A , Isat : 3A



OCP=12A
Iccmax= 200mA
TDC=140mA
Murata. 2.7mm×2.2mmX1.2mm
DCR: 460m Ohm
Idc : 0.85A , Isat : 1A



MULTI BOM

緯創資通

Wistron Corporation

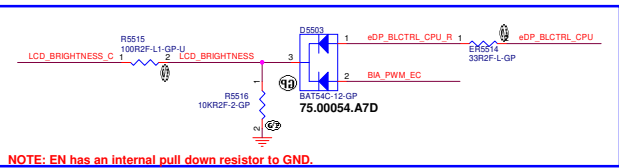
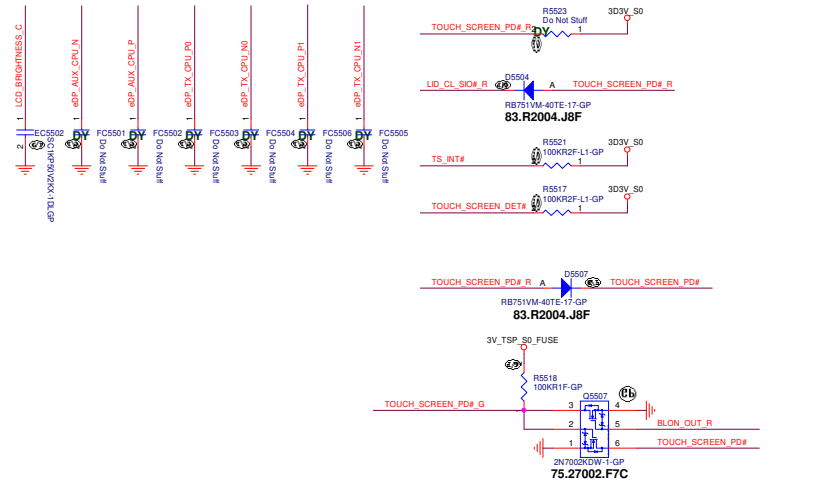
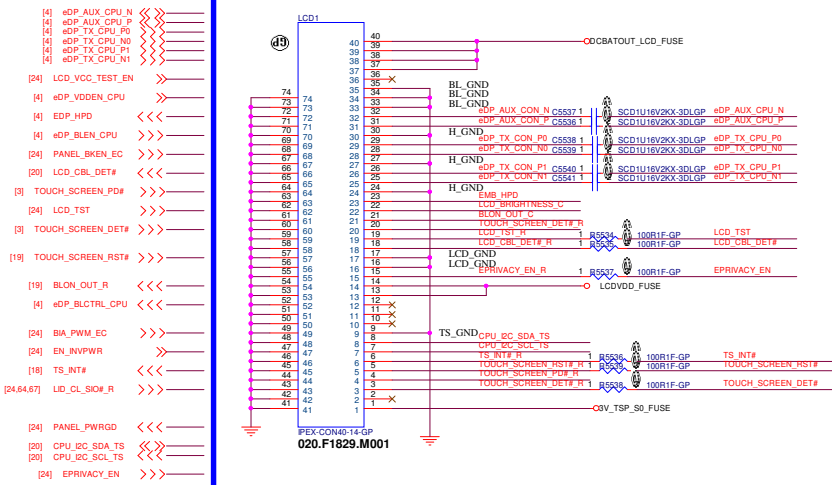
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title **APW8743C_ByPASS**

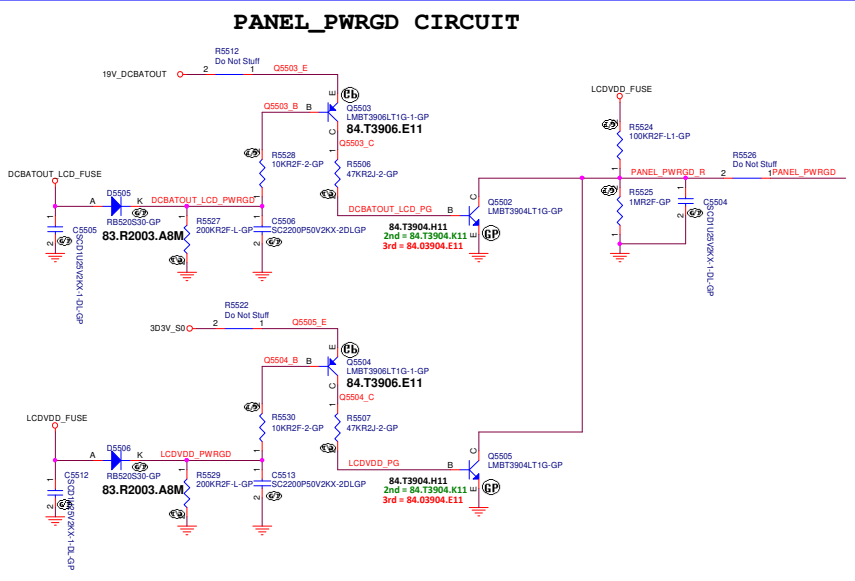
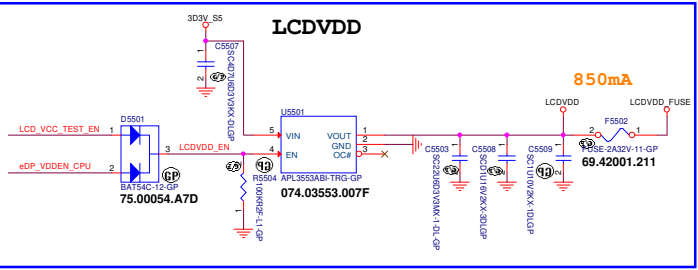
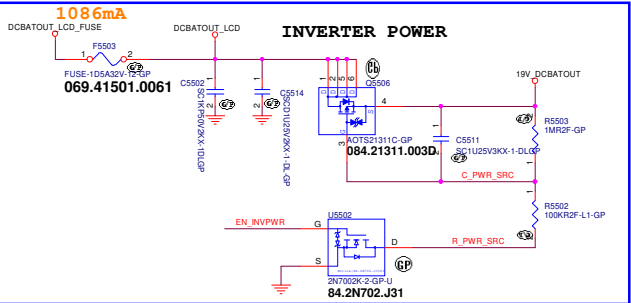
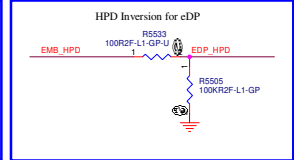
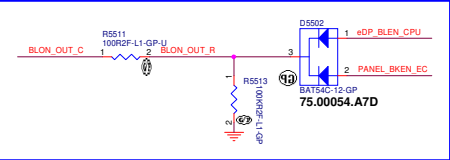
Size A4 Document Number **SouthPeak13 TGL** Rev **A00**

Date: Wednesday, October 28, 2020 Sheet 54 of 106

Main Func = LCD/Touch

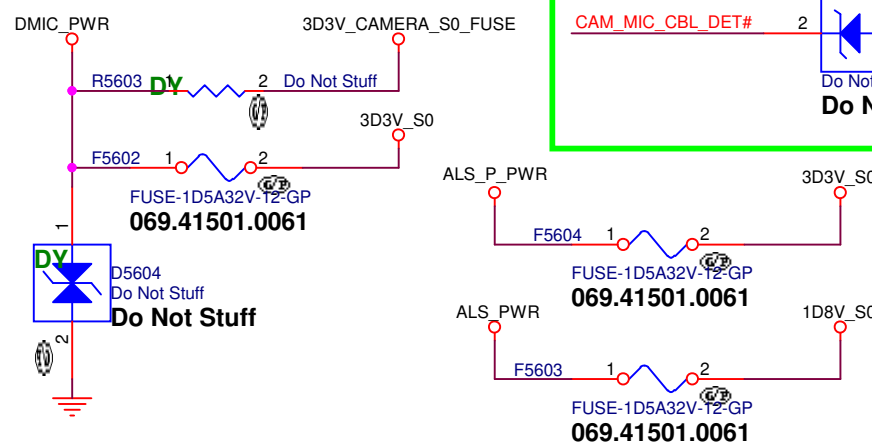
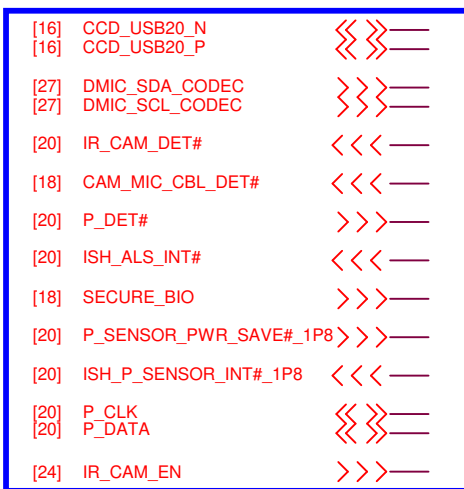
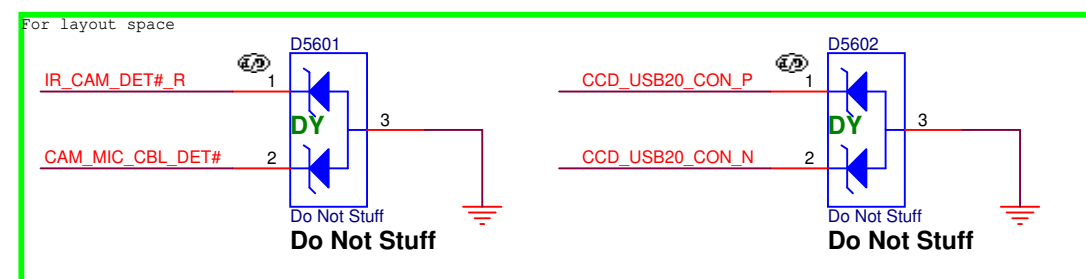
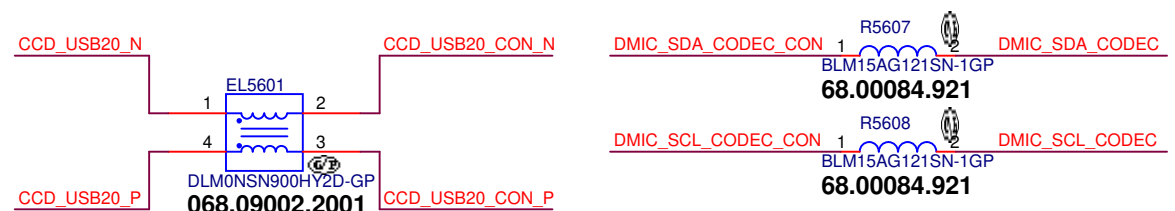
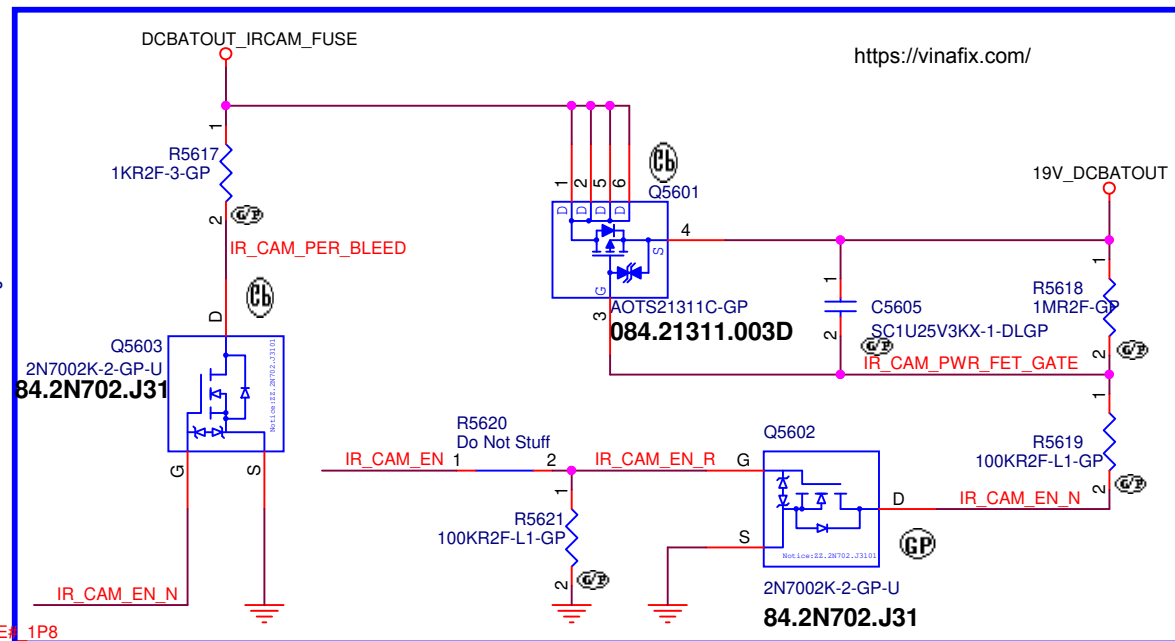
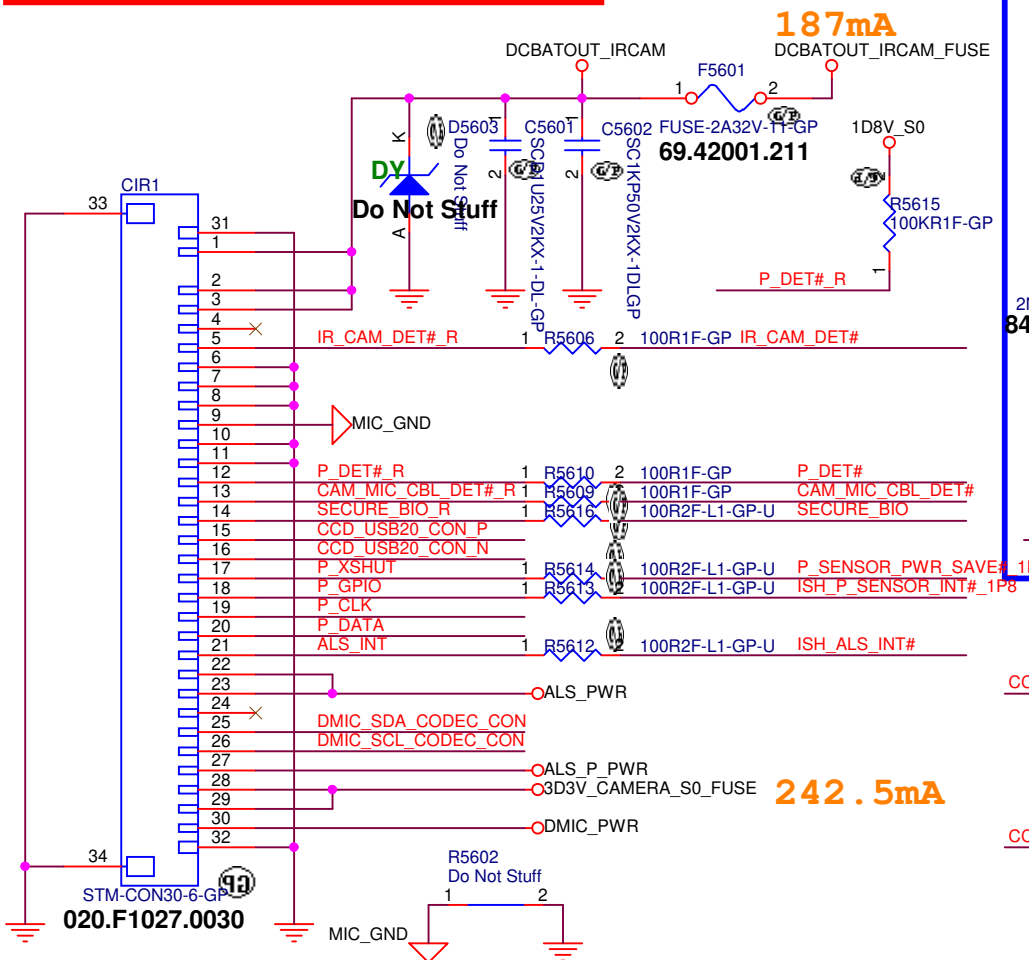


NOTE: EN has an internal pull down resistor to GND.



<https://vinafix.com/>

Main Func = IR CAM



MULTI BOM



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Display (LCD/Inverter)

Size
A4

Document Number

Rev
A00

Date: Wednesday, October 28, 2020

Sheet 56 of 106

5

4

3

2

1

D

D

C

C


B

B

A

A

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Display (RSVD) DP			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 58 of	106

5


4

3


2

1

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Display (RSVD) DVI			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 59 of	106

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD)(HDD)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 60 of	106

Main Func = WLAN

WLAN

[16] WLAN_PCIE_RX_N
[16] WLAN_PCIE_RX_P
[16] WLAN_PCIE_TX_N
[16] WLAN_PCIE_TX_P

BT

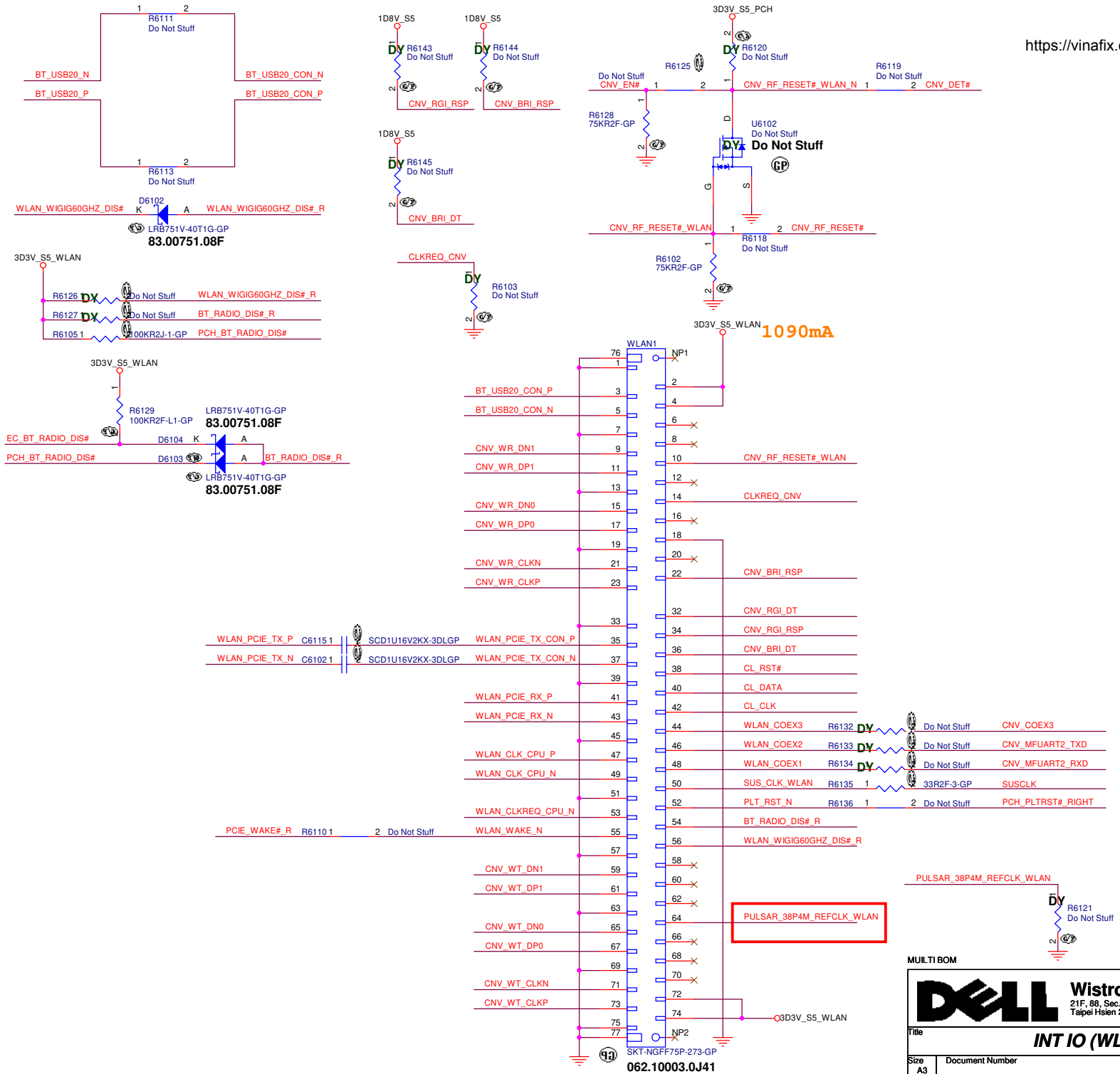
[16] BT_USB20_N   
[16] BT_USB20_P   

CNVi

[21]	CNV_WR_DN1	<<<<	—
[21]	CNV_WR_DP1	<<<<	—
[21]	CNV_WR_DN0	<<<<	—
[21]	CNV_WR_DP0	<<<<	—
[21]	CNV_WR_CLKN	<<<<	—
[21]	CNV_WR_CLKP	<<<<	—
[21]	CNV_WT_DN1	>>>>	—
[21]	CNV_WT_DP1	>>>>	—
[21]	CNV_WT_DN0	>>>>	—
[21]	CNV_WT_DP0	>>>>	—
[21]	CNV_WT_CLKN	>>>>	—
[21]	CNV_WT_CLKP	>>>>	—
[21]	CNV_BRI_RSP	<<<<	—
[21]	CNV_RGL_DT	<<<<	—
[21]	CNV_BRI_DT	<<<<	—
[21]	CNV_RGL_RSP	<<<<	—
[19]	CNV_RF_RESET#	<<<<	—
[24]	CNV_DET#	>>>>	—

WLAN

[18]	WLAN_CLK_CPU_P	<<<	>>>
[18]	WLAN_CLK_CPU_N	<<<	>>>
[18]	WLAN_CLKREQ_CPU_N	<<<	>>>
62.63	PCIE_WAKE#_R	>>>	<<<
21.62	CNV_COEX3	<<<	>>>
20.62	CNV_MFUART2_TXD	<<<	>>>
20.62	CNV_MFUART2_RXD	<<<	>>>
[18]	CL_CLK	<<<	>>>
[18]	CL_DATA	<<<	>>>
[18]	CL_RST#	<<<	>>>
[19]	CLKREQ_CNV	>>>	<<<
[24]	WLAN_WIGIG60GHz_DIS#	>>>	<<<
[24]	EC_BT_RADIO_DIS#	>>>	<<<
18.63	SUSCLK	>>>	<<<
32.91	PCH_PLTRST#_RIGHT	>>>	<<<
[19]	CNV_EN#	>>>	<<<
[19]	PCH_BT_RADIO_DIS#	>>>	<<<



<https://vinafix.com/>

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

INT IO (WLAN M.2)Size
A3

Document Number

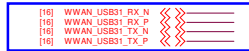
Rev	
A00	

Date: Wednesday, October 28, 2020

Sheet 61 of 106

NGFF(WWAN/SSD)

WWAN



WWAN



WWAN

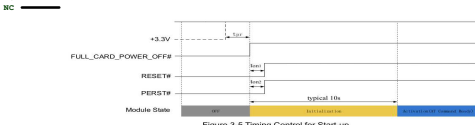
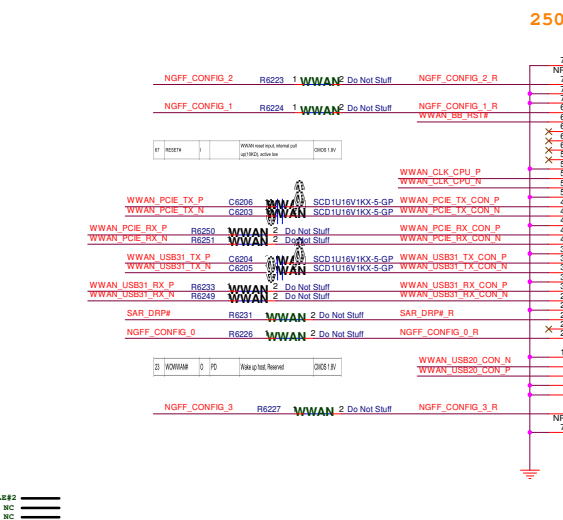
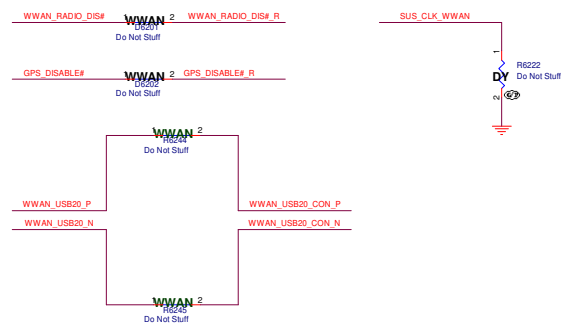
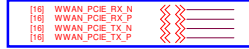


Figure 3-5 Timing Control for Start-up

Index	Minimum	Typical	Notes
t _{pr}	-	-	+3.3V power supply rises time. If power supply always ready, there is no t _{pr}
t _{on1}	10ms	30ms	If the RESET# has a residual voltage, then 30ms is necessary
t _{on2}	10ms	30ms	PERST# should de-asserted after FULL_CARD_POWER_OFF#

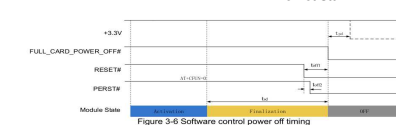
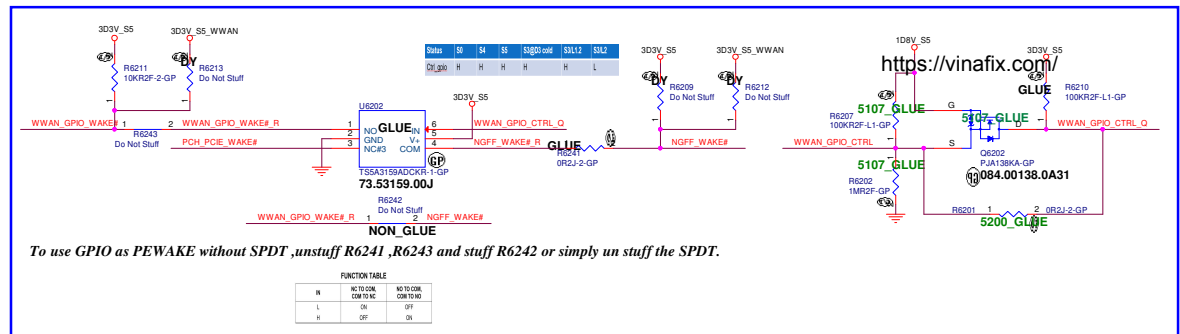
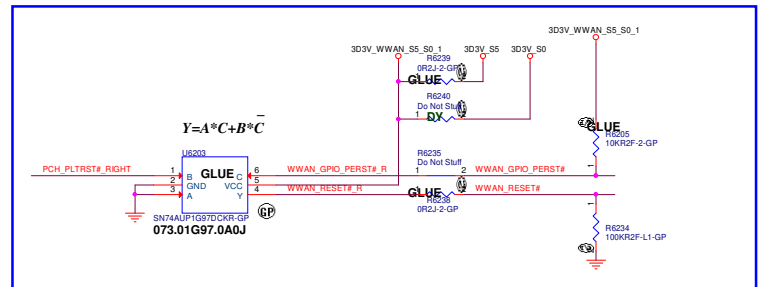


Figure 3-6 Software control power

Index	Minimum	Typical	Maxim	Notes
t _{pd}	10ms	100ms	-	+3.3V power supply goes down time. If power supply is always on, there is no t _{pd}
t _{off1}	10ms	30ms	-	RESET# should asserted before FULL_CARD_POWER_OFF
t _{off2}	0ms	30ms	t _{off1}	PERST# should asserted after RESET#



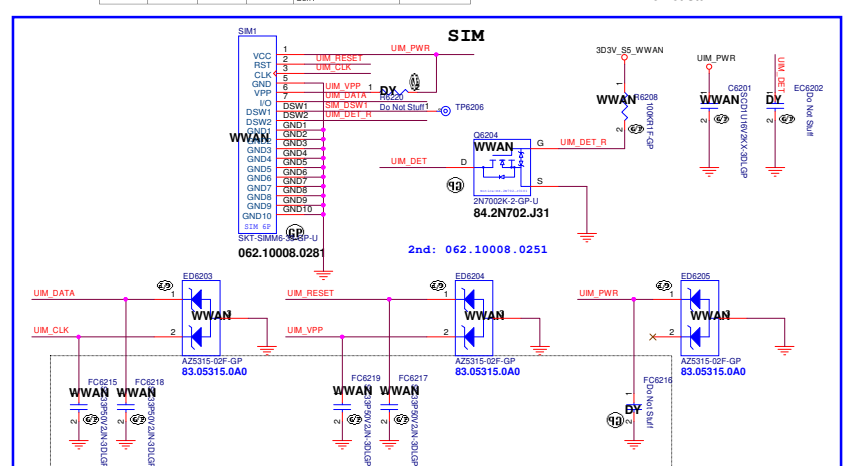
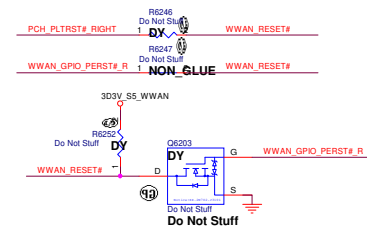
IN	NC TO COM, COM TO NC	NO TO COM, COM TO NO
L	ON	OFF
H	OFF	ON



STATE#	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type	M0042_CONFIG_STATE
0	GND	GND	GND	GND	SSD-SATA	High
1	GND	HIGH	GND	GND	SSD-PCIe2 (lane)	Low
8	HIGH	GND	GND	GND	WWAN	Low
14	HIGH	GND	HIGH	HIGH	HCA-PCIe1 (lane)	Low
15	HIGH	HIGH	HIGH	HIGH	NA	Low

The M.2 module configuration as the following table

Config_0 (pin21)	Config_1 (pin69)	Config_2 (pin75)	Config_3 (pin1)	Module Type and Main Host Interface	Port Configuratio
GND	GND	GND	NC	WWAN-USB3.1, PCIe Gen1	0



Layout Close to SIM1 Connector

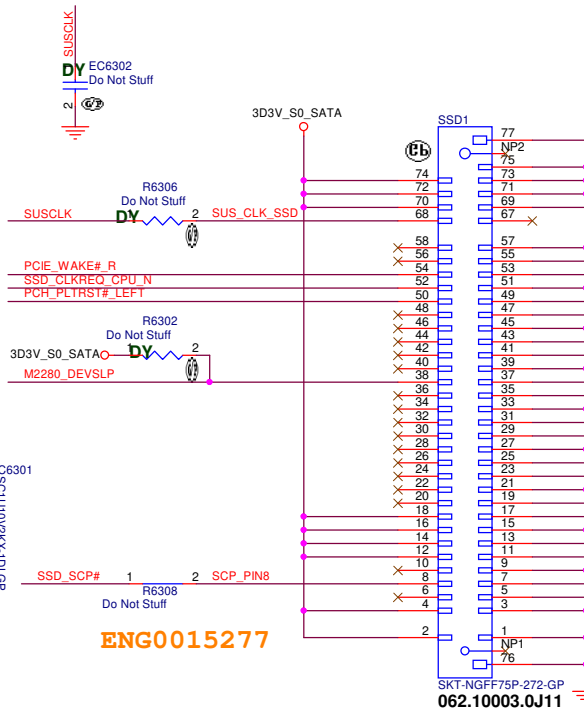
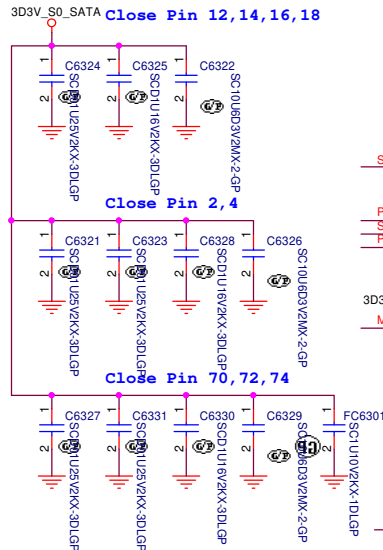
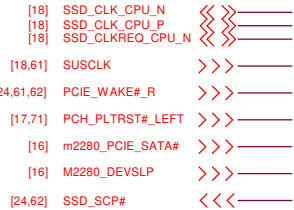
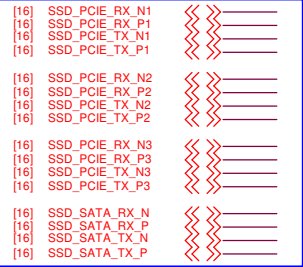
MULTI BOM

Title **INT IO WWAN**

Size A2	Document Number	Rev A0
Date: Wednesday, October 28, 2020	Sheet 62 of	106

Main Func = m.2 SSD

SSD



PEDET	0	Host I/F Indication: To be grounded for SATA, No Open-drain for PCIe	OVINC
L		SATA	
H		PCIe	

SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values					
Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2 / SATA	PCI Express* Gen 3 / SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ¹

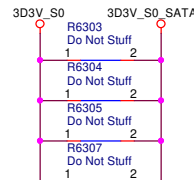
74	3.3V	GND	75
72	3.3V	GND	73
70	3.3V	GND	71
68	SUSCLK(32kHz) (O)(0/3.3V)	PEDET (NC-PCIe/GND-SATA)	69
	Connector Key	N/C	67
	Connector Key		
	Connector Key		
	Connector Key		
	Connector Key		
58	N/C	GND	57
56	N/C	REFCLKP	55
54	PEWAKE# (I/O)(0/3.3V) or N/C	REFCLKN	53
52	CLKREQ# (I/O)(0/3.3V) or N/C	GND	51
50	PERST# (O)(0/3.3V) or N/C	PETp0/SATA-A+	49
48	N/C	PETn0/SATA-A-	47
46	N/C	GND	45
44	N/C	PERp0/SATA-B-	43
42	N/C	PERn0/SATA-B+	41
40	N/C	GND	39
38	DEVSUP (O)	PETp1	37
36	N/C	PETn1	35
34	N/C	GND	33
32	N/C	PERp1	31
30	N/C	PERn1	29
28	N/C	GND	27
26	N/C	PETp2	25
24	N/C	PETn2	23
22	N/C	GND	21
20	N/C	PERp2	19
18	3.3V	PERn2	17
16	3.3V	GND	15
14	3.3V	PETp3	13
12	3.3V	PETn3	11
10	DAS/DSS# (I/O)/LED1# (I)(0/3.3V)	GND	9
8	N/C	PERp3	7
6	N/C	PERn3	5
4	3.3V	GND	3
2	3.3V	GND	1

6.5.4.6

PCH PCI Express* Controller Lane Reversal

For each PCH PCIe* Controller we support end-to-end lane reversal across the four lanes mapped to a controller for the following two motherboard PCIe* configurations

2800mA



MULTI BOM

**Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

INT IO (SSD M.2/ eMMC)

Size

A3

Document NumberRev

A00

Date

Wednesday, October 28, 2020

Sheet

63

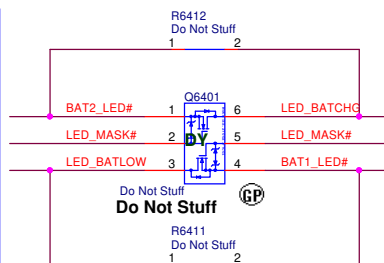
of

106

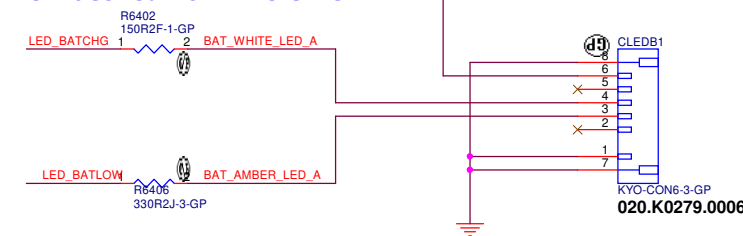
Main Func = LED/HALL/Button

<https://vinafix.com/>

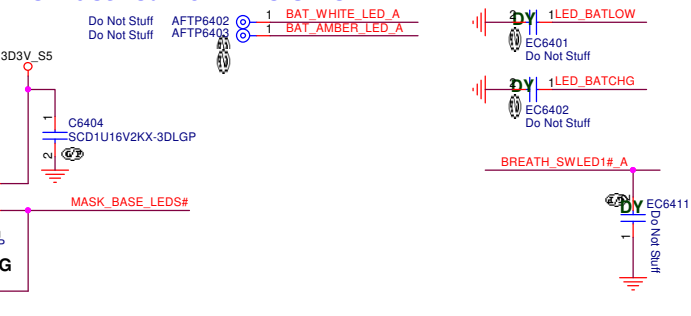
[24] BAT2_LED# >>>
 [24] BAT1_LED# >>>
 [24] LED_MASK# >>>
 [24,68] KBC_PWRBTN# <<<
 [24,55,67] LID_CL_SIO#_R <<<
 [24,67] LID_CL_SIO_TAB#_R >>>
 [24] BREATH_LED# <<<
 [24] FPR_LED# <<<
 [24,92] FPR_DET# >>>
 [24] M_BIST >>>
 [24,44] ACAV_IN >>>
 [17,24,99] RSMRST#_KBC >>>
 [92] FPR_LED_1 <<<
 [92] FPR_LED_2 <<<
 [92] FPR_LED_3 <<<
 [92] FPR_LED_4 <<<



Battery LED2(White LED) LOW acted from KBC GPIO



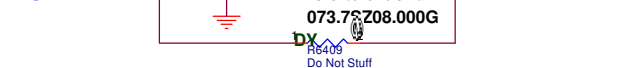
Battery LED1(Orange LED) LOW acted from KBC GPIO



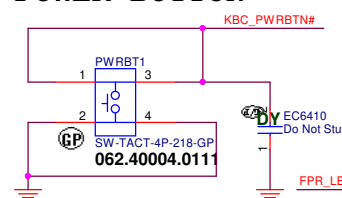
OTHER



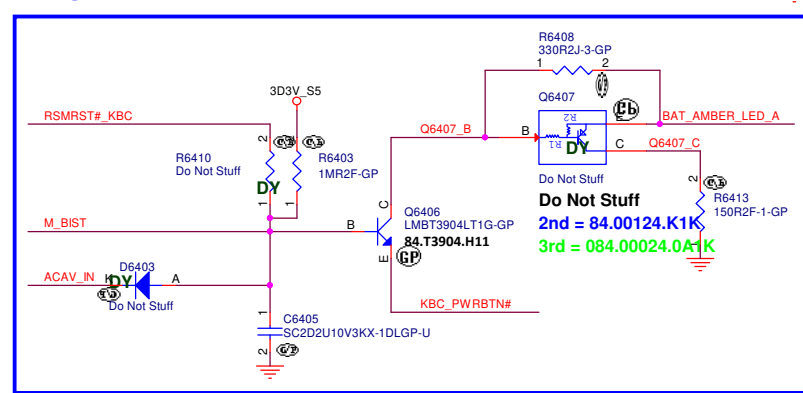
POWERBT



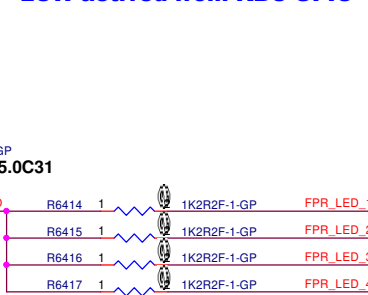
POWER BUTTON



M-BIST



Power LED LOW acted from KBC GPIO



MULTI BOM

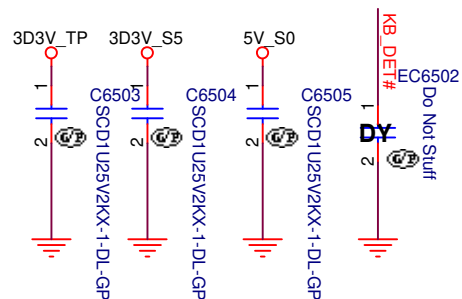
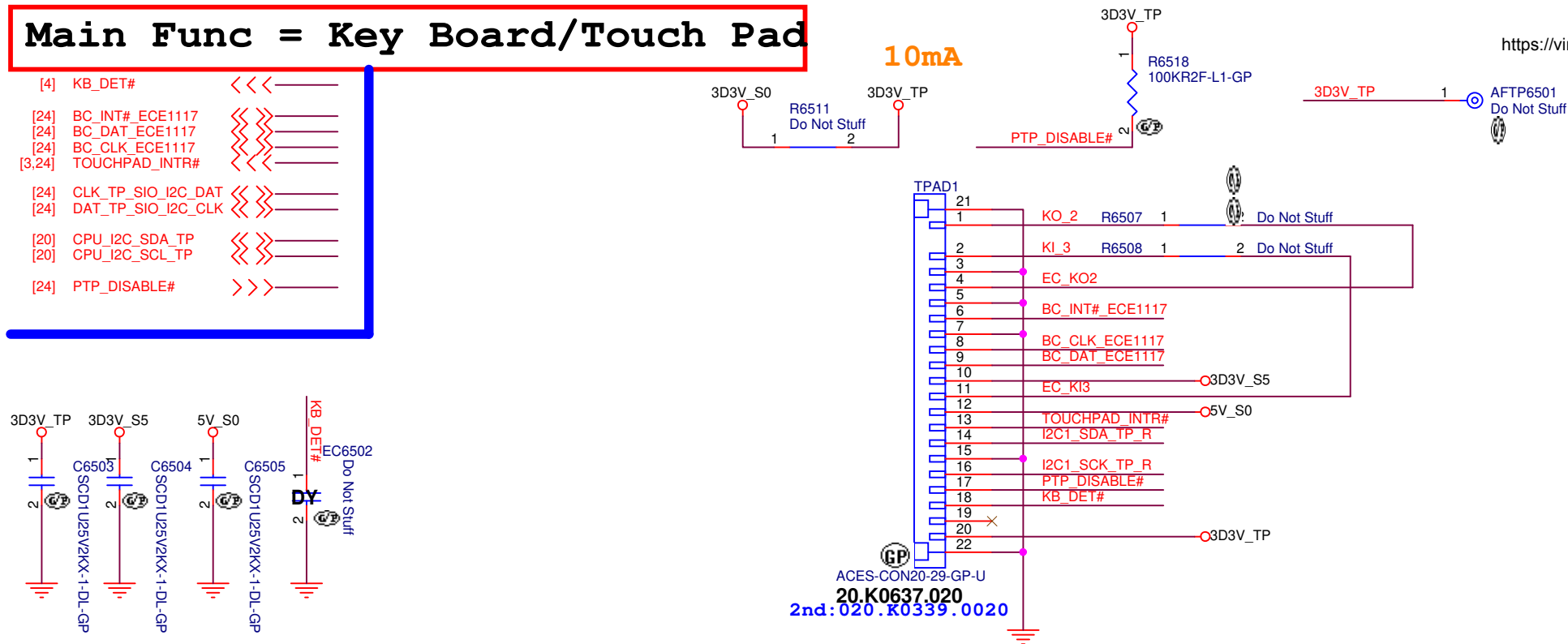
DELL		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichin, Taipei Hsien 221, Taiwan, R.O.C.	
Title LED / Button / Power Button			
Size Custom	Document Number	Rev A00	
Date: Wednesday, October 28, 2020		Sheet 64	of 106

Main Func = Key Board/Touch Pad

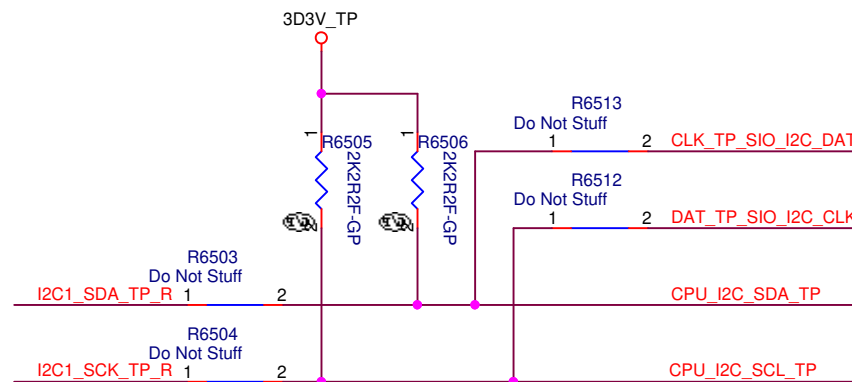
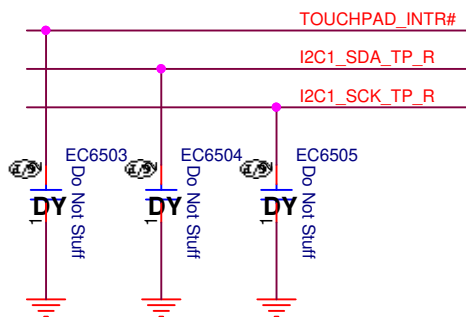
[4]	KB_DET#	<<<	---
[24]	BC_INT#_ECE1117	<<<	---
[24]	BC_DAT_ECE1117	<<<	---
[24]	BC_CLK_ECE1117	<<<	---
[3,24]	TOUCHPAD_INTR#	<<<	---
[24]	CLK_TP_SIO_I2C_DAT	<<<	---
[24]	DAT_TP_SIO_I2C_CLK	<<<	---
[20]	CPU_I2C_SDA_TP	<<<	---
[20]	CPU_I2C_SCL_TP	<<<	---
[24]	PTP_DISABLE#	>>>	---

10mA

<https://vinafix.com/>



ACES-CON20-29-GP-U
20.K0637.020
2nd:020.K0339.0020



MULTI BOM



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

INT IO (KB/TP)

Size
A4

Document Number

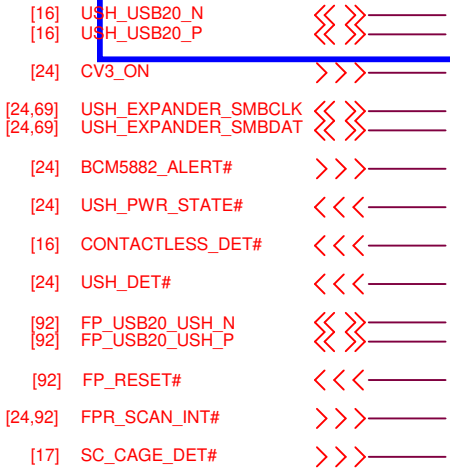
Rev
A00

Date: Wednesday, October 28, 2020

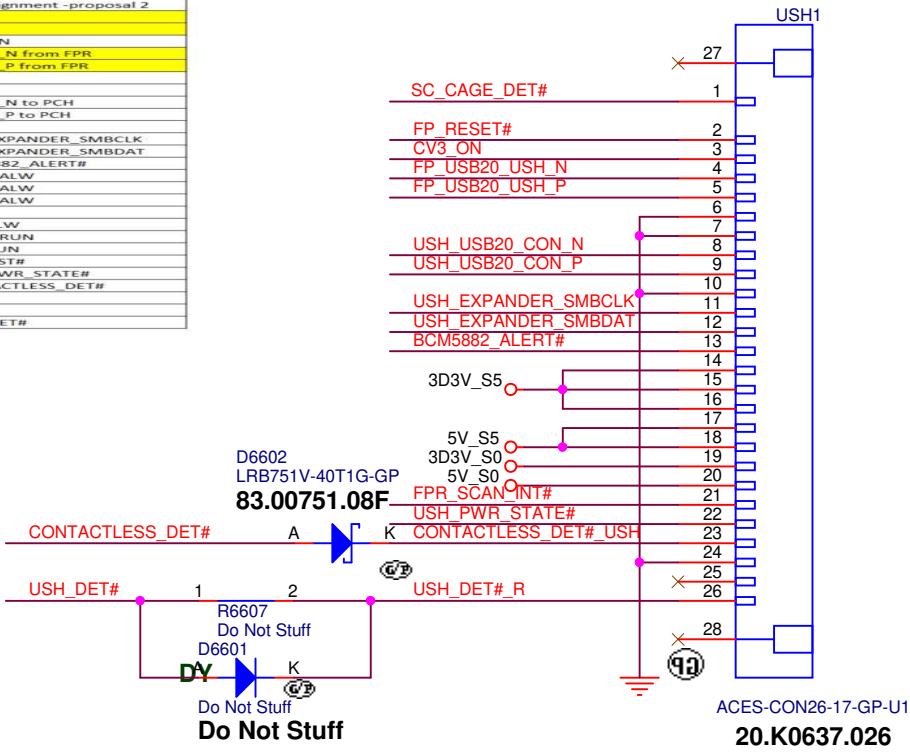
Sheet 65 of 106

Main Func = USH BD

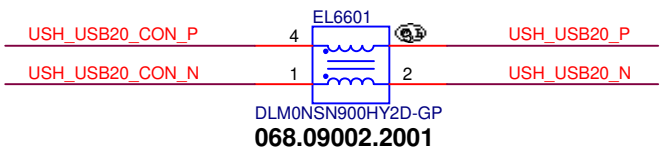
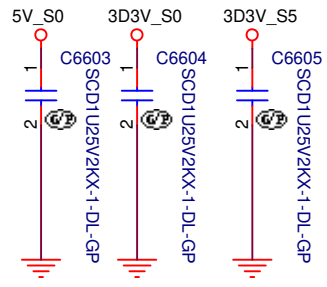
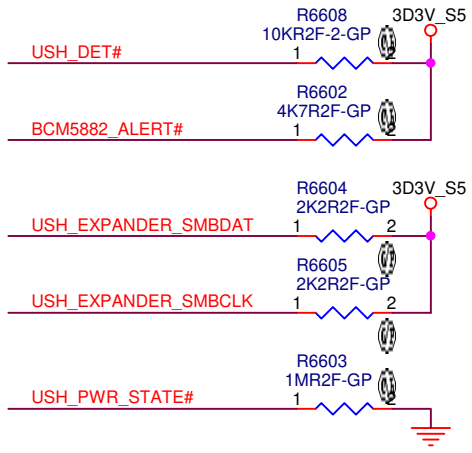
USH




CV3 module	
pin assignment -proposal 2	
NC	
NC	
CV2_ON	
USB20_N from FPR	
USB20_P from FPR	
GND	
GND	
USB20_N to PCH	
USB20_P to PCH	
GND	
USH_EXPANDER_SMBCLK	
USH_EXPANDER_SMBDAT	
BCM5882_ALERT#	
+3.3V_ALW	
+3.3V_ALW	
+3.3V_ALW	
NC	
+5V_ALW	
+3.3V_RUN	
+5V_RUN	
USH_RST#	
USH_PWR_STATE#	
CONTACTLESS_DET#	
GND	
GND	
USH_DET#	



https://vinafix.com/



MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **IO Board Conn (USH)**

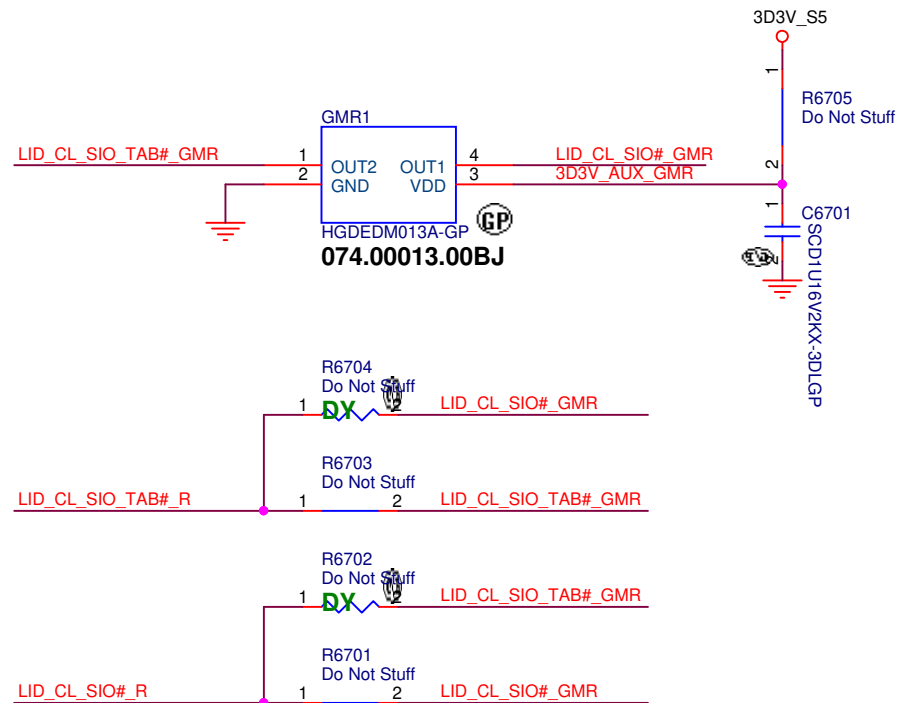
Size A4	Document Number	Rev A00
Date: Wednesday, October 28, 2020		Sheet 66 of 106

Main Func = Sensor (Hall-Sensor)

<https://vinafix.com/>

[24,55,64] LID_CL_SIO#_R << >>—

[24] LID_CL_SIO_TAB#_R << >>—



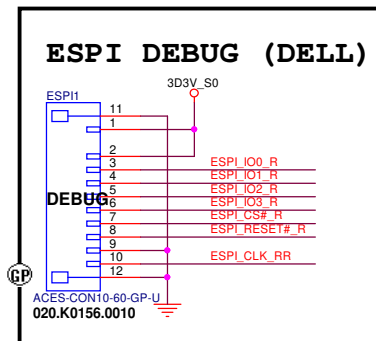
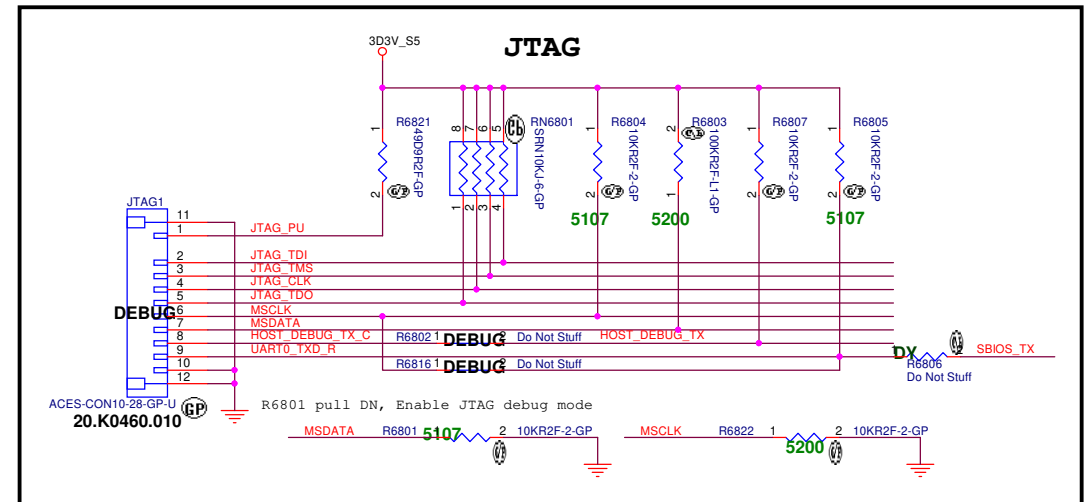
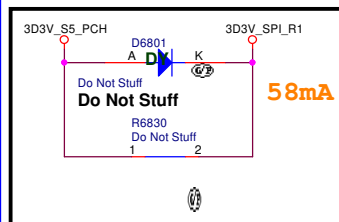
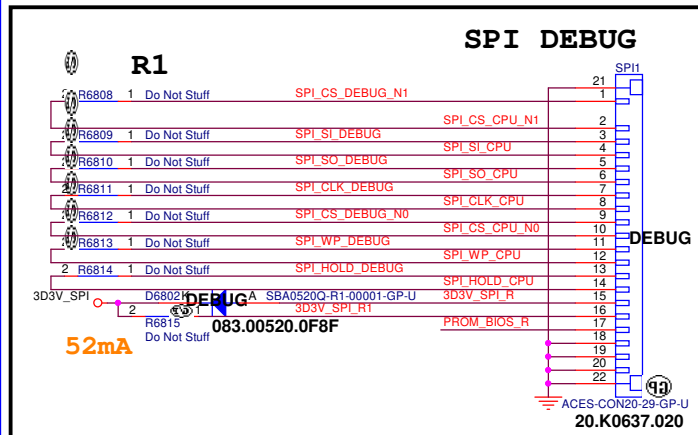
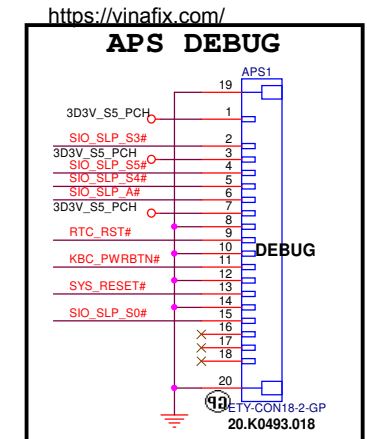
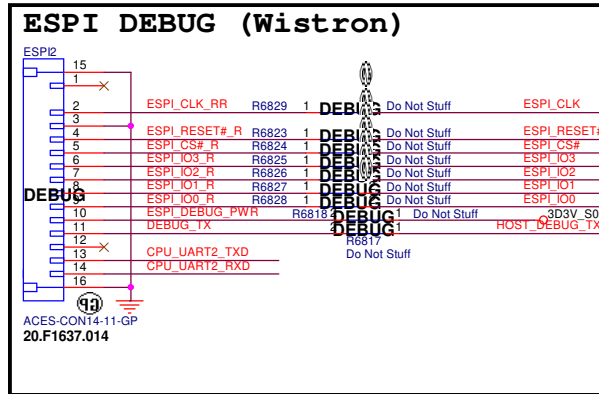
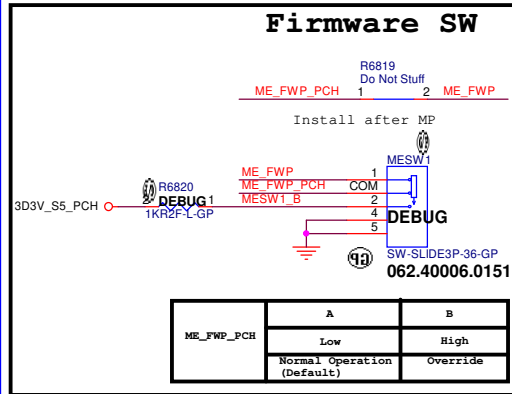
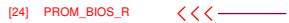
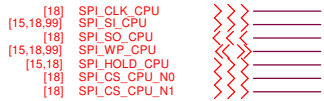
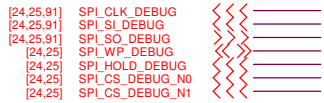
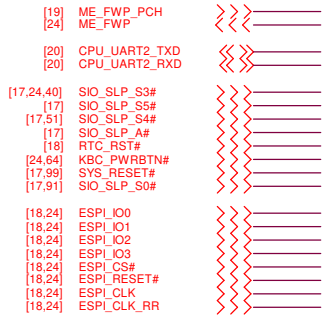
MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

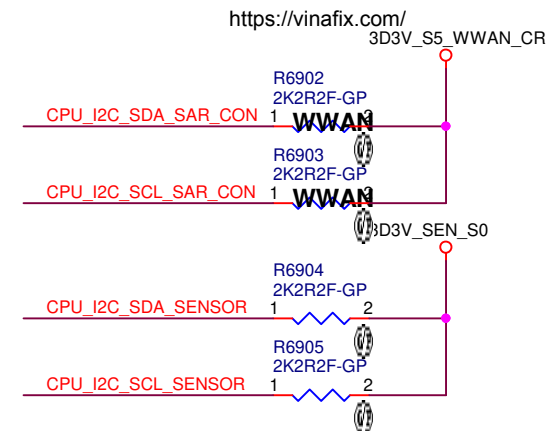
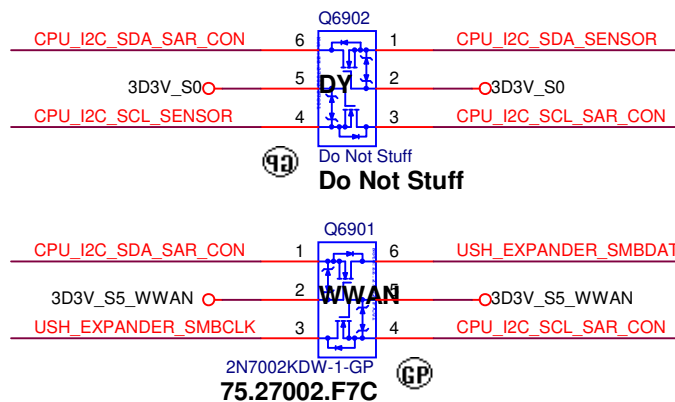
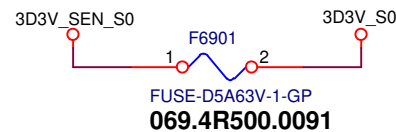
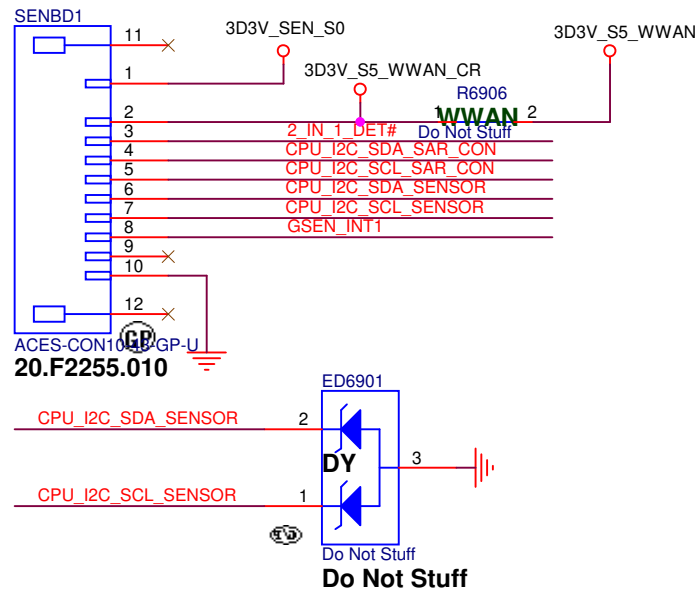
Title			Sensor (Hall-Sensor)		
Size	Document Number				Rev
A4					A00
Date: Wednesday, October 28, 2020			Sheet	67	of 106

Main Func = Debug



Main Func = Sensor (E-compass/A+Gyro/SAR)

[20]	GSEN_INT1	<<<_____
[20,70]	CPU_I2C_SDA_SENSOR	<<<>>>_____
[20,70]	CPU_I2C_SCL_SENSOR	<<<>>>_____
[24,66]	USH_EXPANDER_SMBDAT	<<<>>>_____
[24,66]	USH_EXPANDER_SMBCLK	<<<>>>_____
[16,24]	2_IN_1_DET#	<<<<_____



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Sensor (GYROSCOPE/PRESSUE/ALS)

Size
A4

Document Number

Rev	A00
-----	------------

Date: Wednesday, October 28, 2020

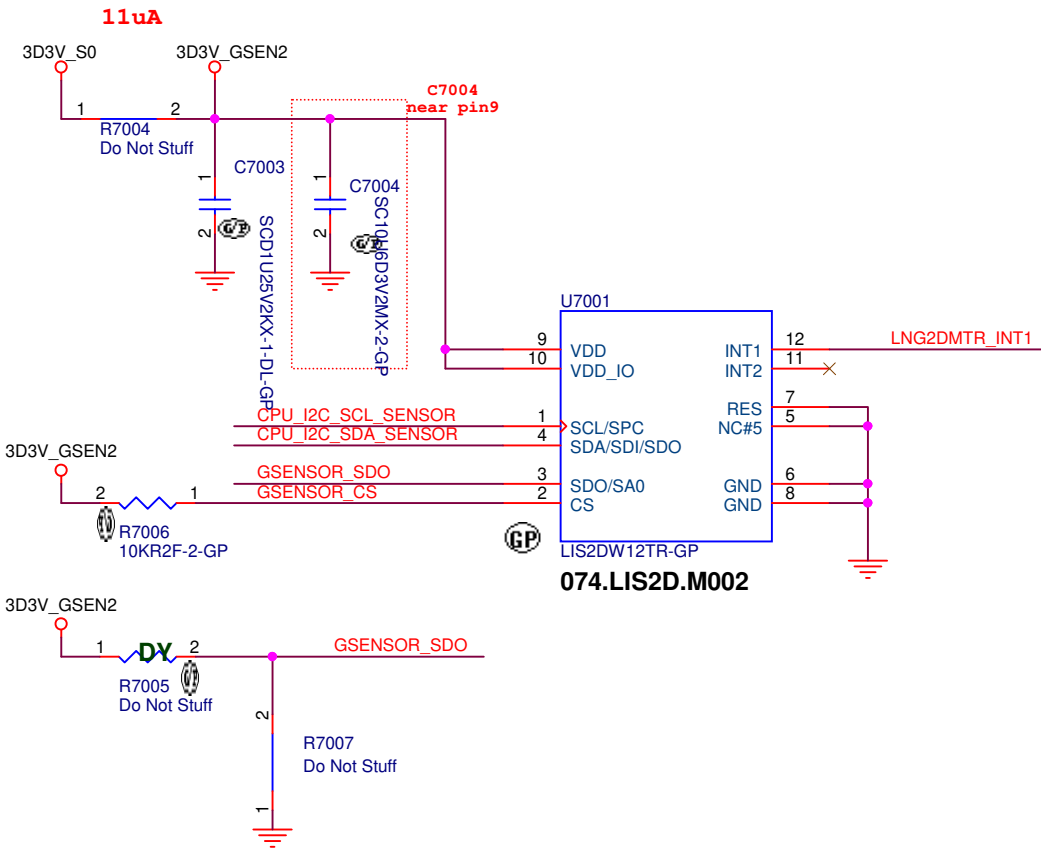
Sheet 69 of 106

Main Func = G-sensor


G Sensor

https://vinafix.com/

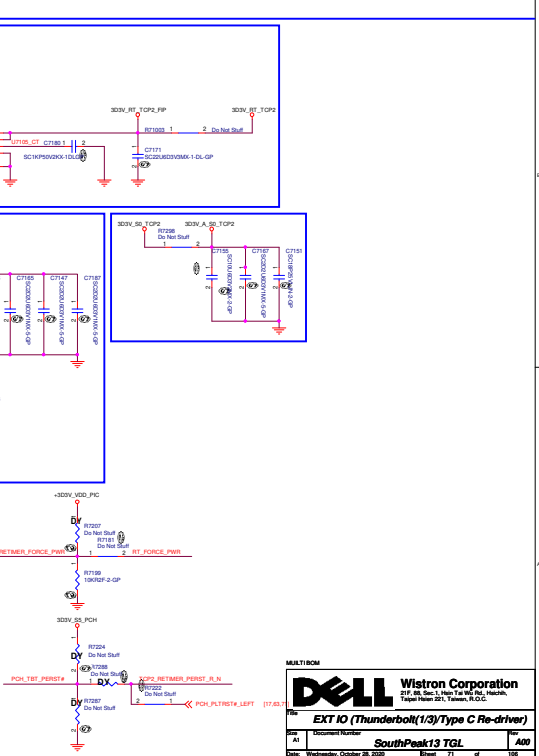
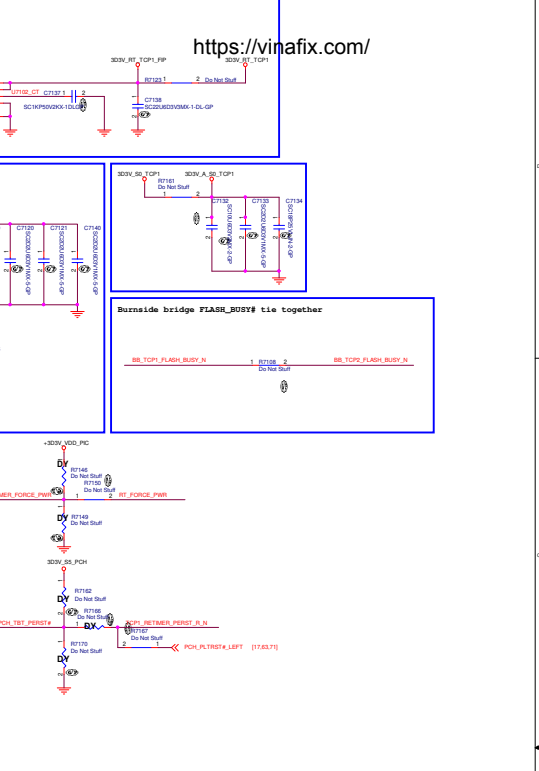
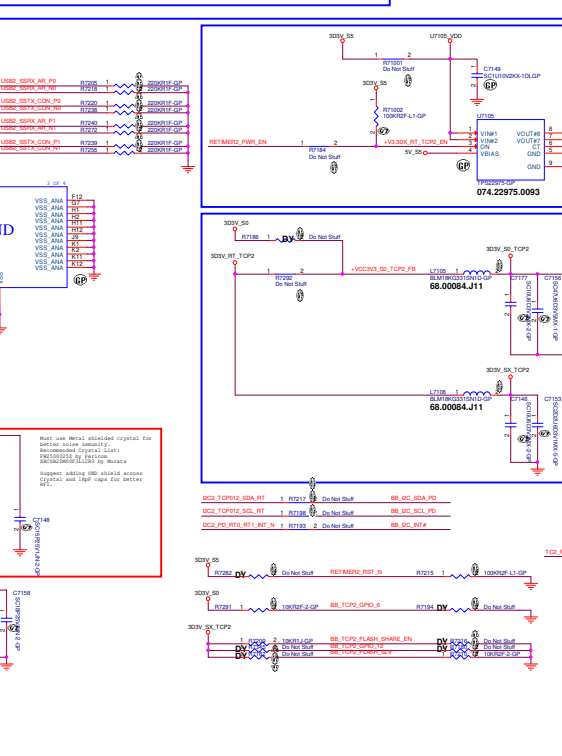
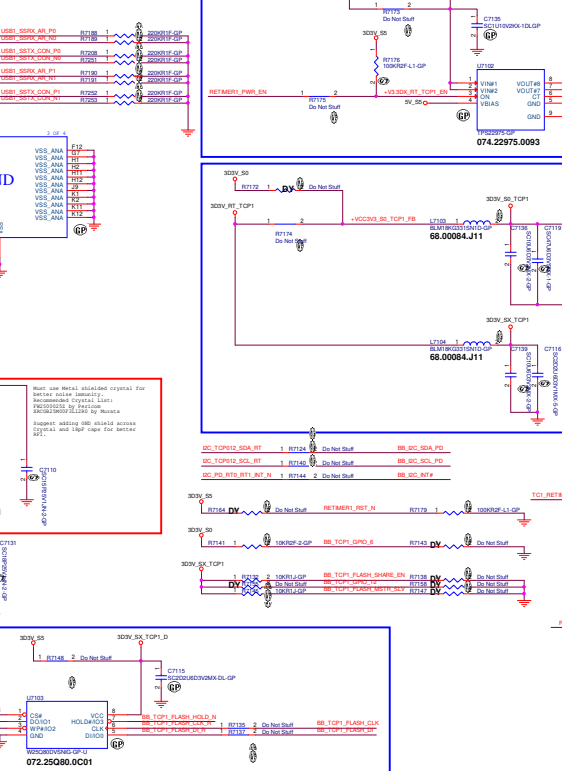
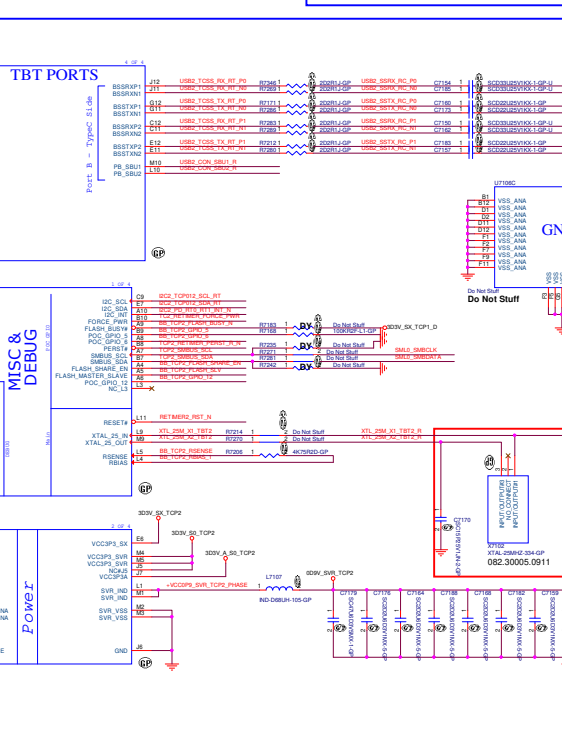
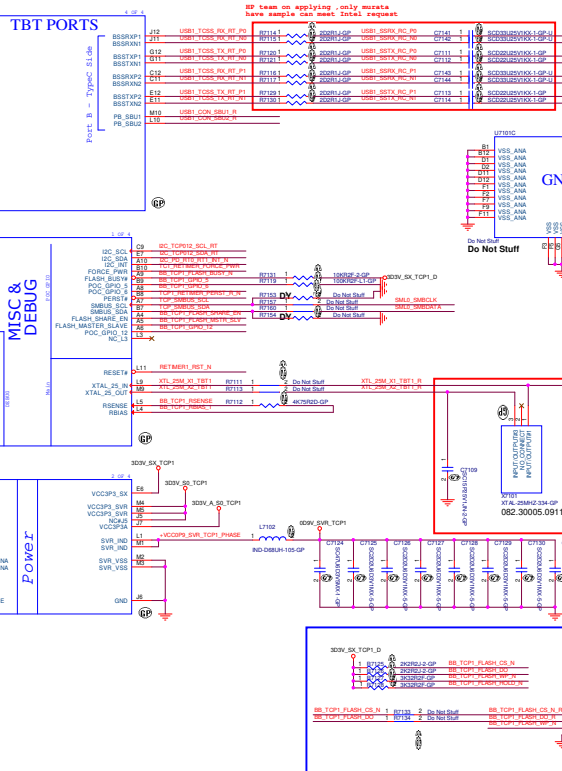
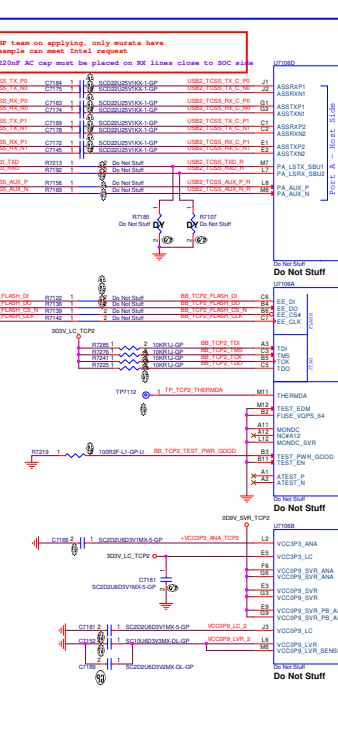
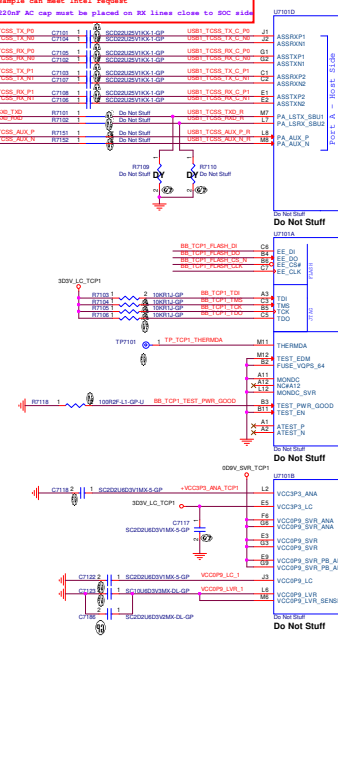
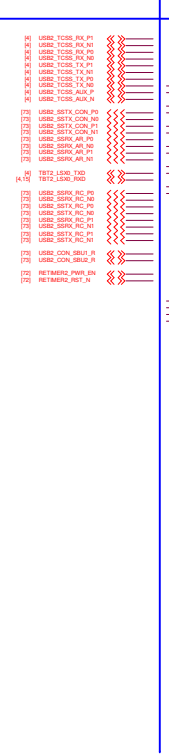
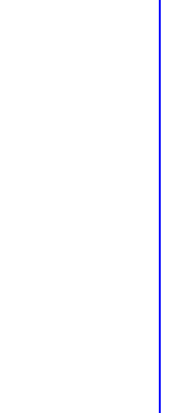
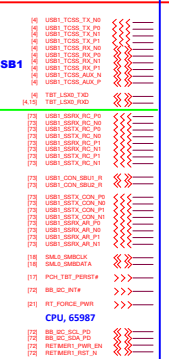
[20,69] CPU_I2C_SDA_SENSOR
[20,69] CPU_I2C_SCL_SENSOR
[20] LNG2DMTR_INT1



MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Sensor (G-sensor)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 70 of	106

Main Func = TBT



https://vinafix.com/

Main Func = TypeC

[24]	UPD1_SMBCLK	>>>>
[24]	UPD1_SMBDAT	>>>>
[24]	UPD1_SMBINT#	>>>>
[73]	USB1_PDA_CC1	>>>>
[73]	USB1_PDA_CC2	>>>>
[74]	EN_PD_HV_1	>>>>
[74]	EN_PD_HV_2	>>>>
[71]	RETIMER1_PWR_EN	>>>>
[71]	RETIMER2_PWR_EN	>>>>
[71]	RETIMER1_RST_N	>>>>
[71]	RETIMER2_RST_N	>>>>
[73]	DDM_MUX1_FLIP_R	>>>>
[73]	DDM_MUX1_EN_R	>>>>
[73]	DDM_MUX1_USB_EN_R	>>>>
[73]	DDM_MUX2_USB_EN_R	>>>>
[3,22,44,46,74]	PROCHOT#_PD_R	>>>>
[73]	USB2_PDB_CC1	>>>>
[73]	USB2_PDB_CC2	>>>>
[71]	BB_I2C_SCL_PD	>>>>
[71]	BB_I2C_SDA_PD	>>>>
[17]	TBT_I2C_INT#	<<<<
[71]	BB_I2C_INT#	<<<<
[73]	DDM_MUX2_FLIP_R	<<<<
[73]	UPD1_SMBCLK_Q	<<<<
[73]	UPD1_SMBDA_Q	<<<<
[18]	SML1_SMBDATA	<<<<
[18]	SML1_SMBCLK	<<<<

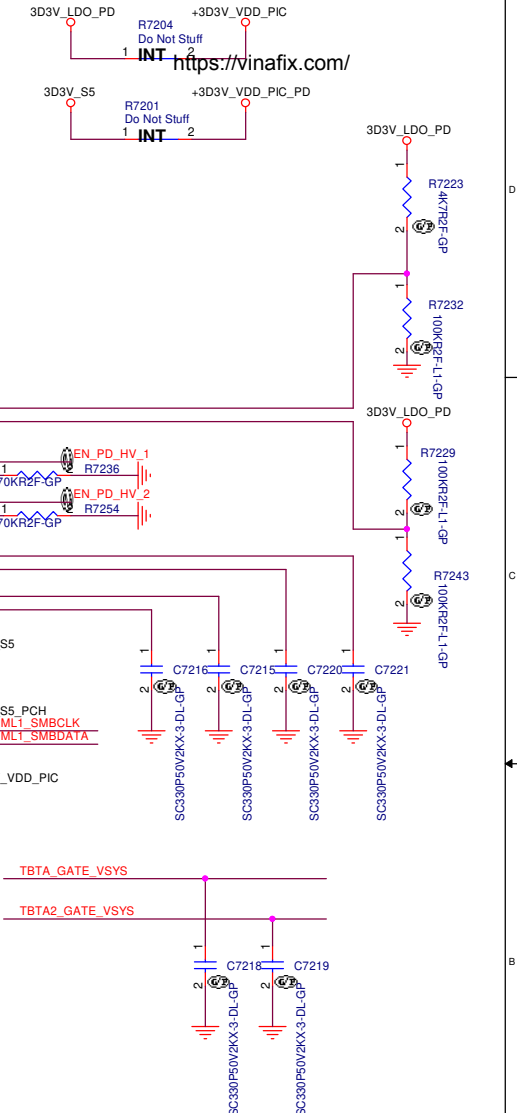
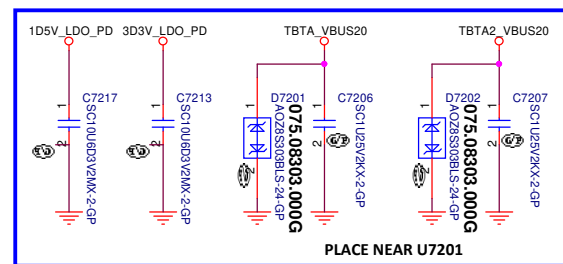
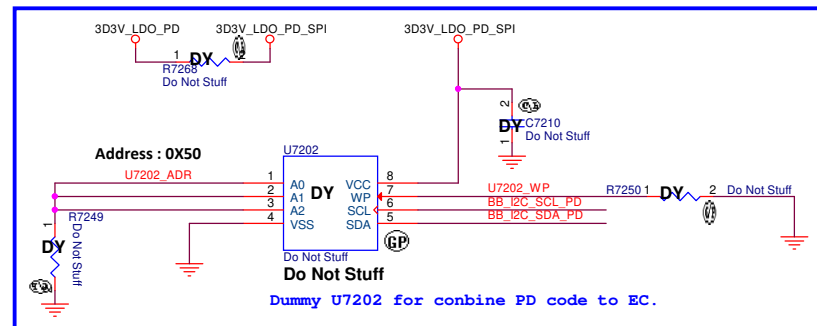
UPD1_SMBDA_Q 1 2 UPD1_SMBDAT

UPD1_SMBCLK 1 2 UPD1_SMBCLK_Q

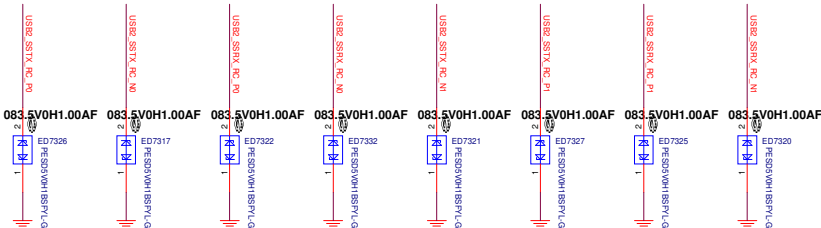
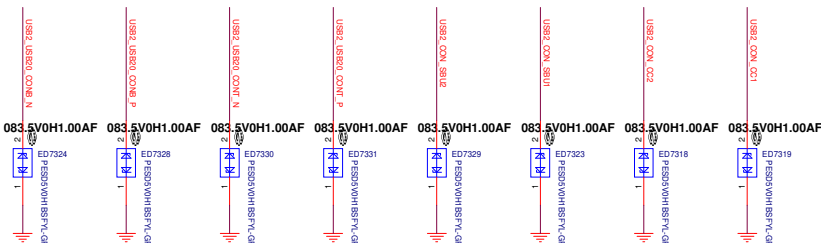
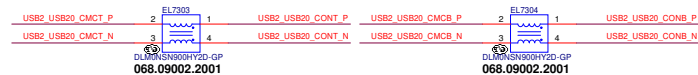
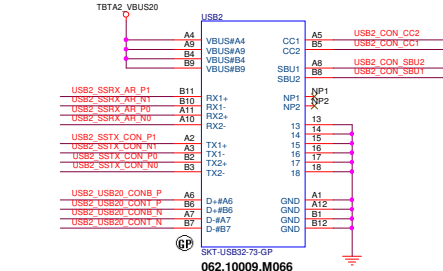
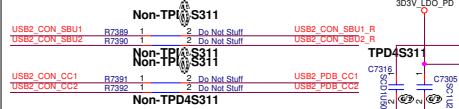
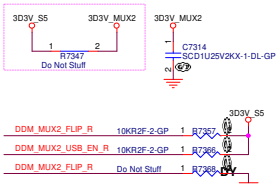
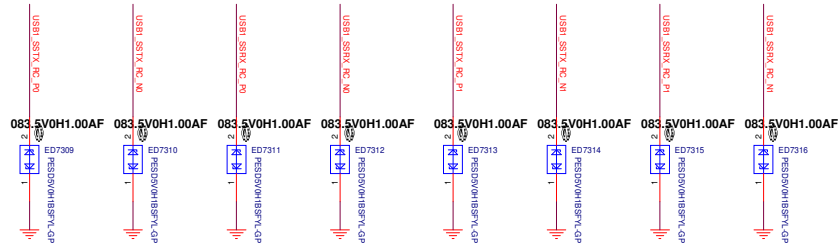
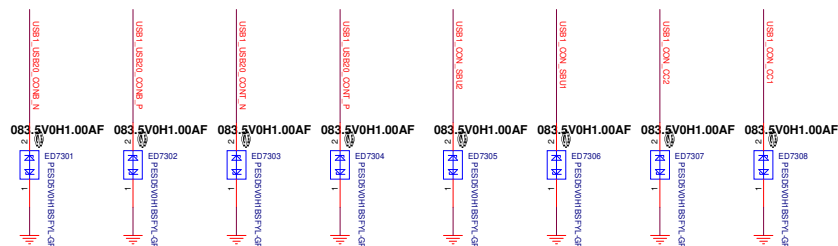
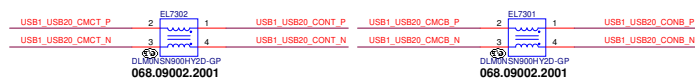
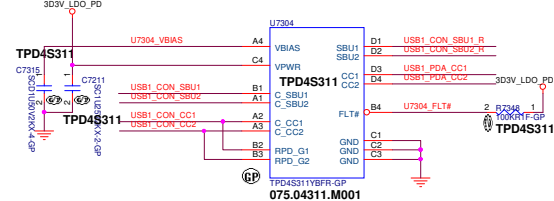
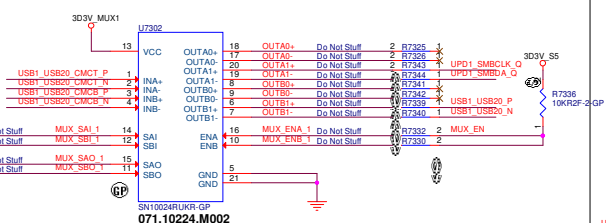
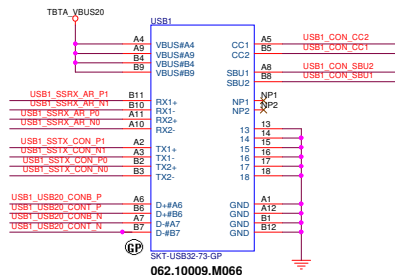
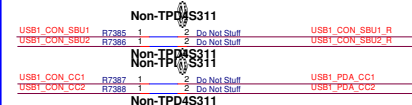
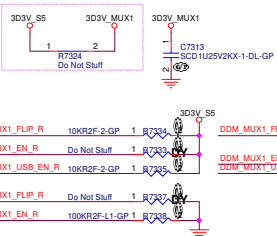
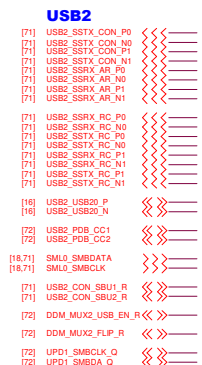
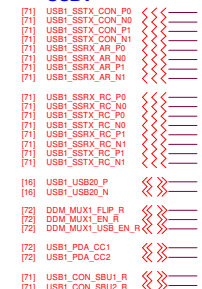
+3D3V_VDD_PIC

1 R7266 2 2K2R2F-GP BB_I2C_SCL_PD

1 R7267 2 2K2R2F-GP BB_I2C_SDA_PD

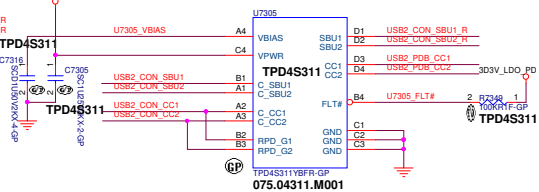


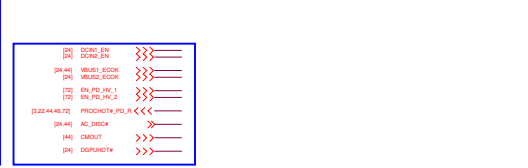
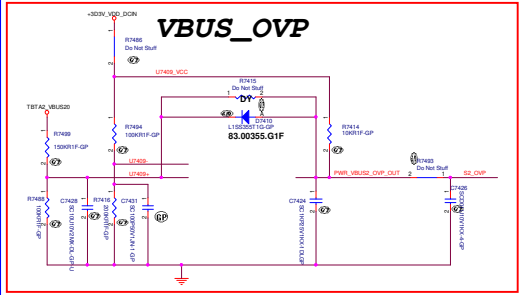
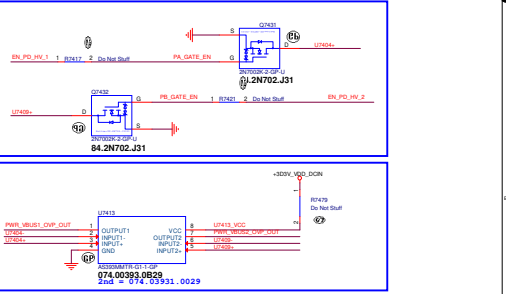
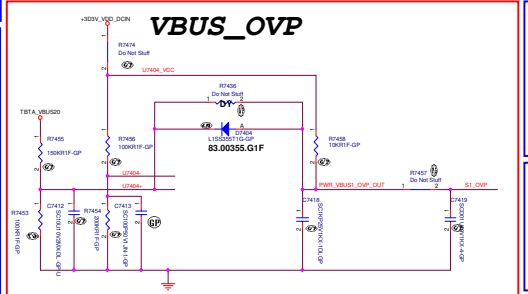
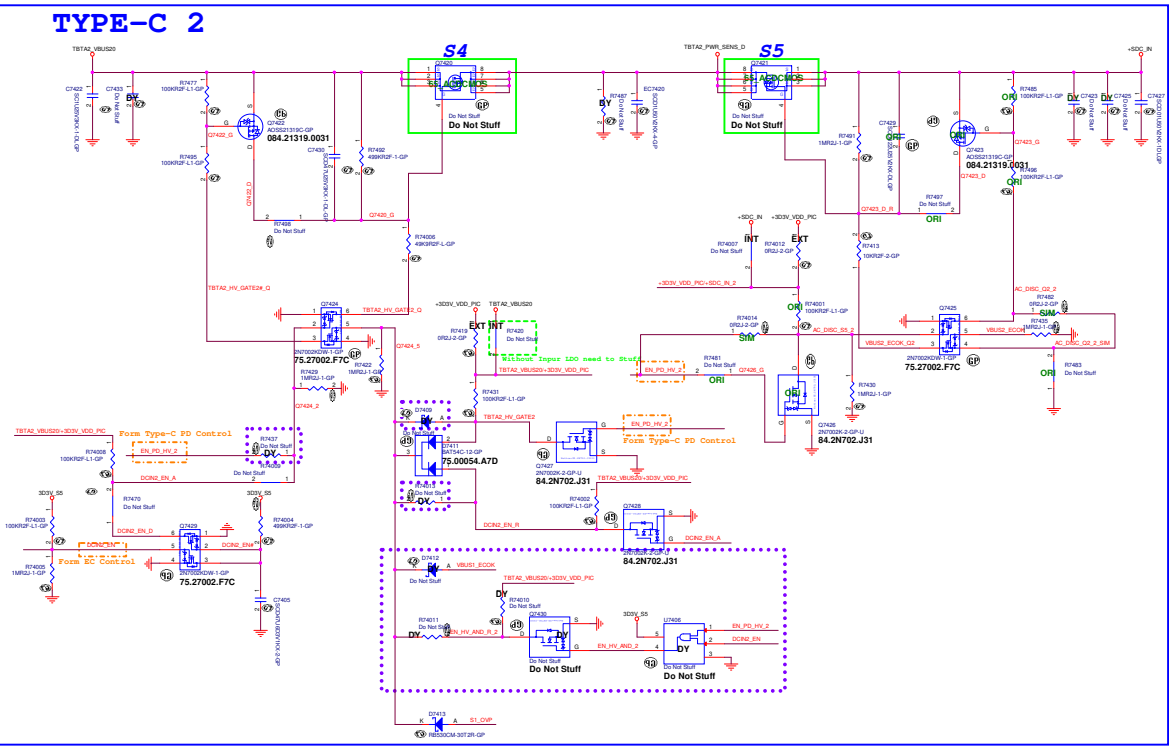
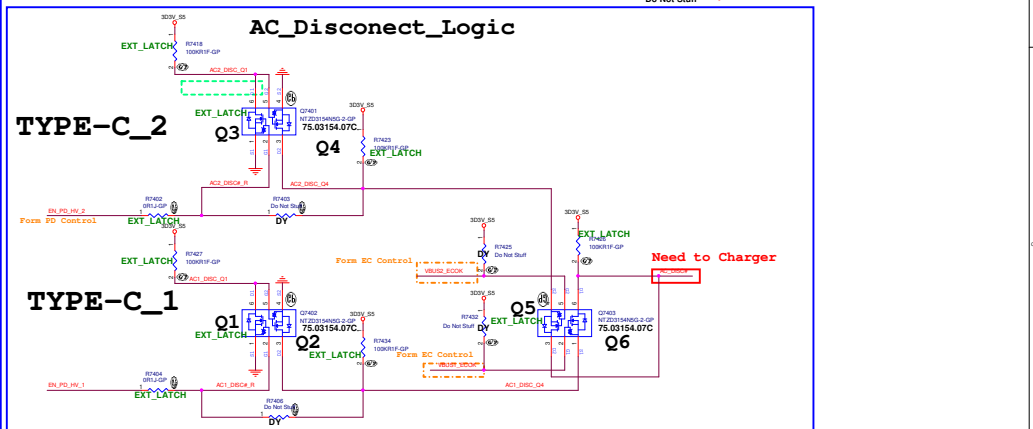
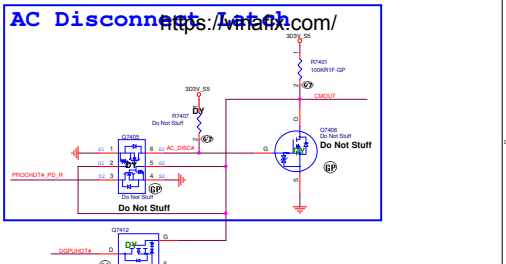
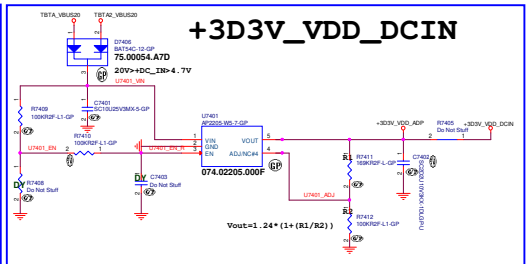
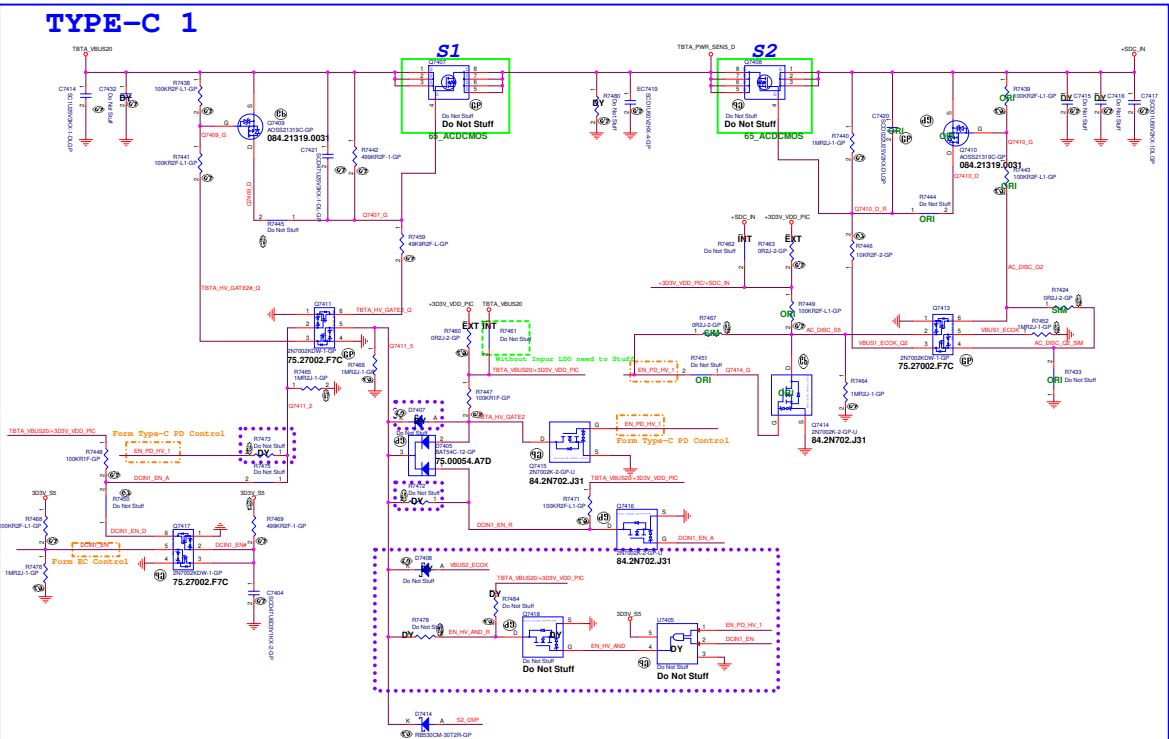
Main Func = TypeC

USB1

<https://vinafix.com/>

PIN DESCRIPTION		TRUTH TABLE		
NAME	DESCRIPTION	S	OE	FUNCTION
OE	Bus-switch enable	X	H	Disconnect
S	Select input	L	L	$D = 1D$
D	Bus A	H	L	$D = 2D$
+D	Bus B			





5

4

3

2

1

D

D

C

C


B

B


A

A

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title EXT IO (RSVD)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 75 of	106

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (RSVD) (PEG 1/5)		
Size A4	Document Number	Rev A00
Date: Wednesday, October 28, 2020		Sheet 76 of 106

5

4

3

2

1

D

D

C

C


B

B


A

A


MULTI BOM

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title GPU (RSVD) (DIGITAL 2/5)					
Size A4		Document Number			Rev A00
Date: Wednesday, October 28, 2020			Sheet 77 of 106		

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title GPU (RSVD) (VRAM 3/5)		
Size A4	Document Number	Rev A00
Date: Wednesday, October 28, 2020		Sheet 78 of 106

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (GPIO 4/5)


Size
A4

Document Number

Rev
A00

Date: Wednesday, October 28, 2020Sheet 79 of 106

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPU (RSVD) (PWR/GND 5/5)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 80 of	106

5

4

3

2

1

<https://vinafix.com/>

D

D

C

C

B

B

A

A

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM1,2 1/4)

Size A4	Document Number	Rev A00
------------	-----------------	-------------------

5

4

3

2

1

<https://vinafix.com/>

D

D

C

C

B

B

A

A

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM3,4 2/4)

Size A4	Document Number	Rev A00
------------	-----------------	-------------------

5

4

3

2

1

D

D

C

C

B

B

A

A

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (VRAM5,6 3/4)

Size A4	Document Number	Rev A00
------------	-----------------	-------------------

5

4

3

2

1

<https://vinafix.com/>

D

D

C

C

B

B

A

A

MULTI BOM




Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title


GPU (RSVD) (VRAM7,8 4/4)

Size A4	Document Number	Rev A00
------------	-----------------	-------------------

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPU (RSVD) (VGA_CORE)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 85 of	106

MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

GPU (RSVD) (Sequence)


Size
A4

Document Number


Rev
A00

Date: Wednesday, October 28, 2020Sheet 86 of 106

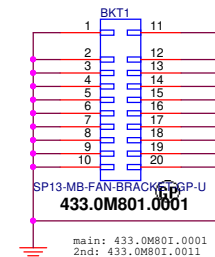
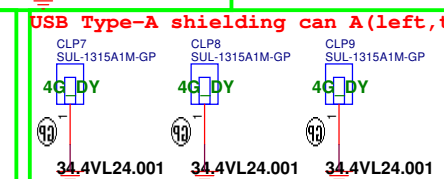
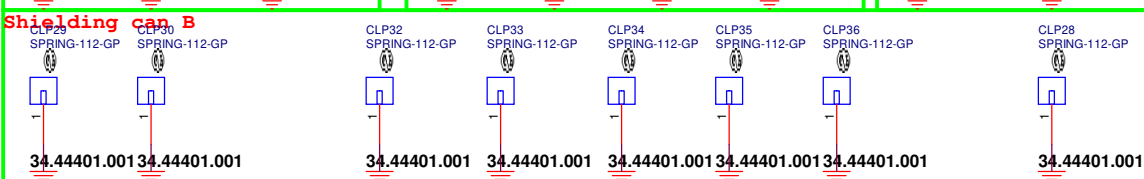
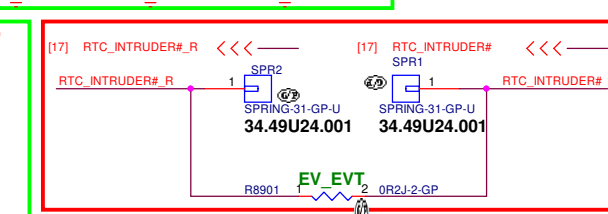
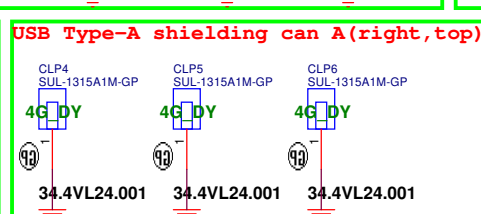
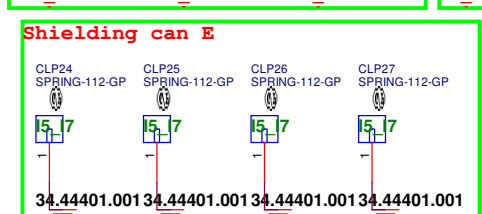
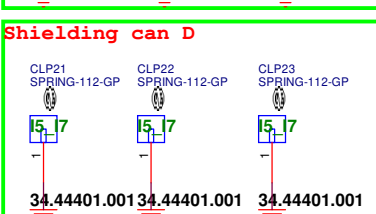
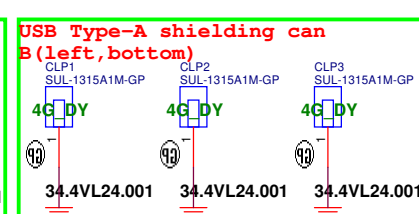
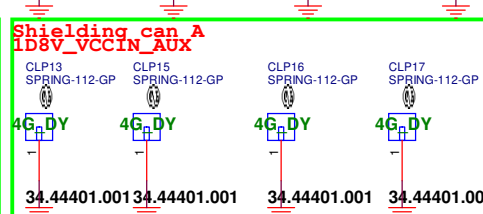
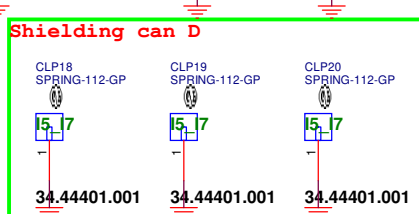
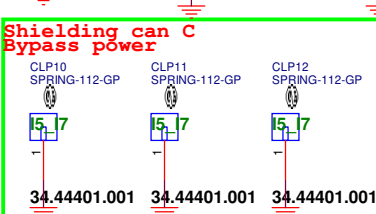
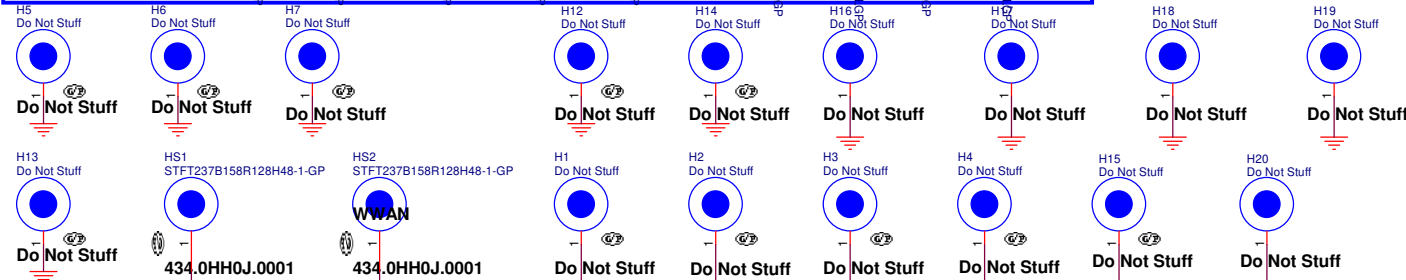
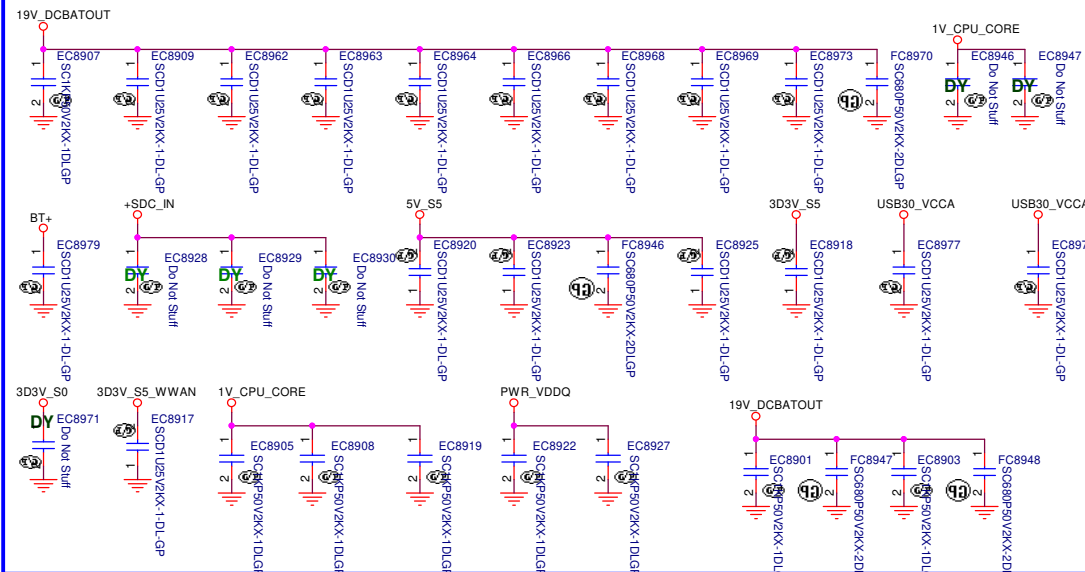
MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title GPU (RSVD)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 87 of	106


MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title UNUSED PARTS (RSVD)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 88 of	106

Main Func = EMC/ RF

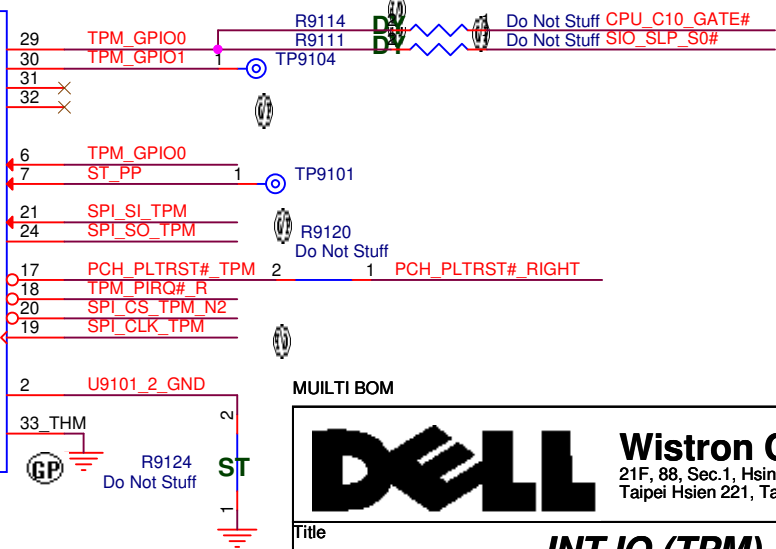
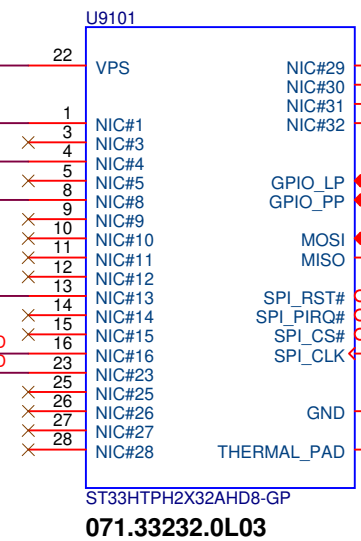
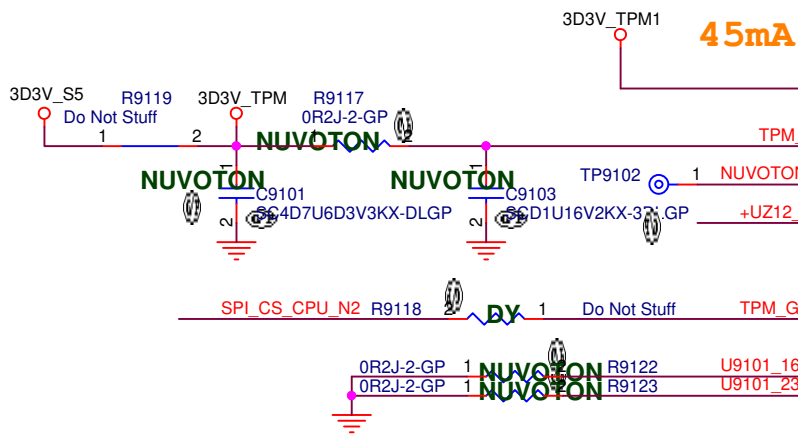
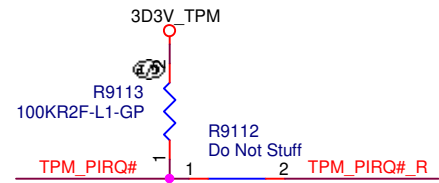
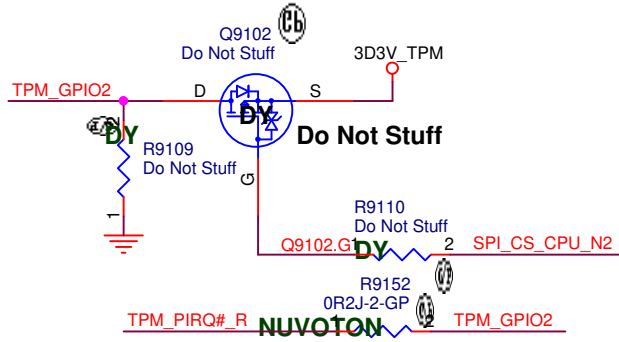
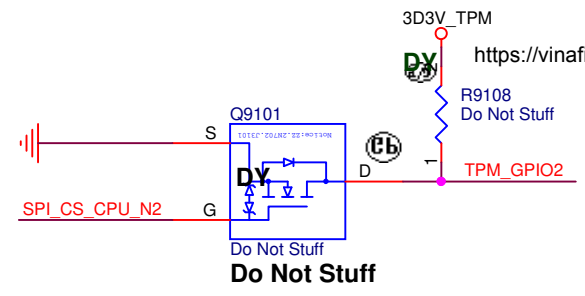
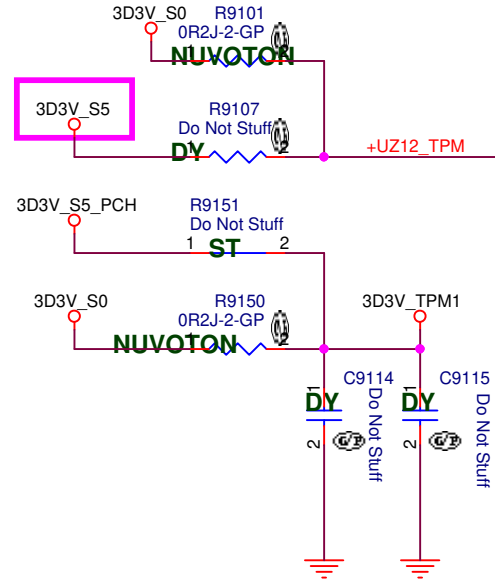
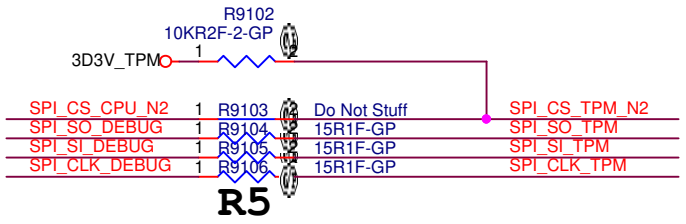
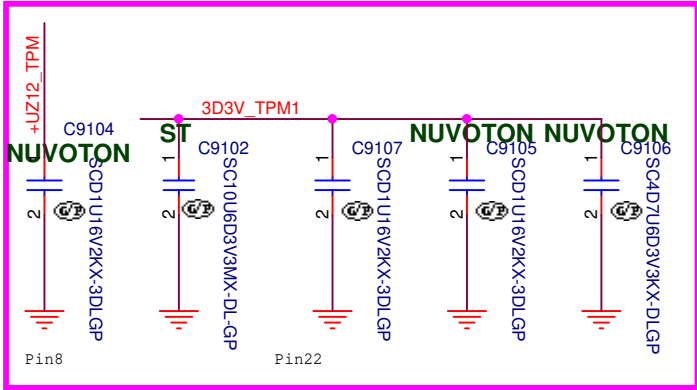


MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title INT IO (RSVD) (NFC)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 90 of	106

Main Func = TPM

- [20] TPM_PIRQ#
- [17,68] SIO_SLP_S0#
- [17,33,61,62] PCH_PLTRST#_RIGHT
- [24,25,68] SPI_CLK_DEBUG
- [24,25,68] SPI_SI_DEBUG
- [24,25,68] SPI_SO_DEBUG
- [18] SPI_CS_CPU_N2
- [17,40] CPU_C10_GATE#



MULTI BOM

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: INT IO (TPM)

Size: A4	Document Number:	Rev: A00
Date: Wednesday, October 28, 2020		Sheet 91 of 106

Main Func = Finger Printer

[24,64] FPR_DET# <<<—

[66] FP_USB20_USH_N <<<—

[66] FP_USB20_USH_P <<<—

[24] FPR_PWR_EN# >>>—

[24,66] FPR_SCAN_INT# <<<—

[24] FPR_SSO_EN# >>>—

[24] FPR_UEFI_MGMT# >>>—

[24] FPR_LOW_PWR_MODE# >>>—

[66] FP_RESET# >>>—

[16] FP_USB20_P <<<—

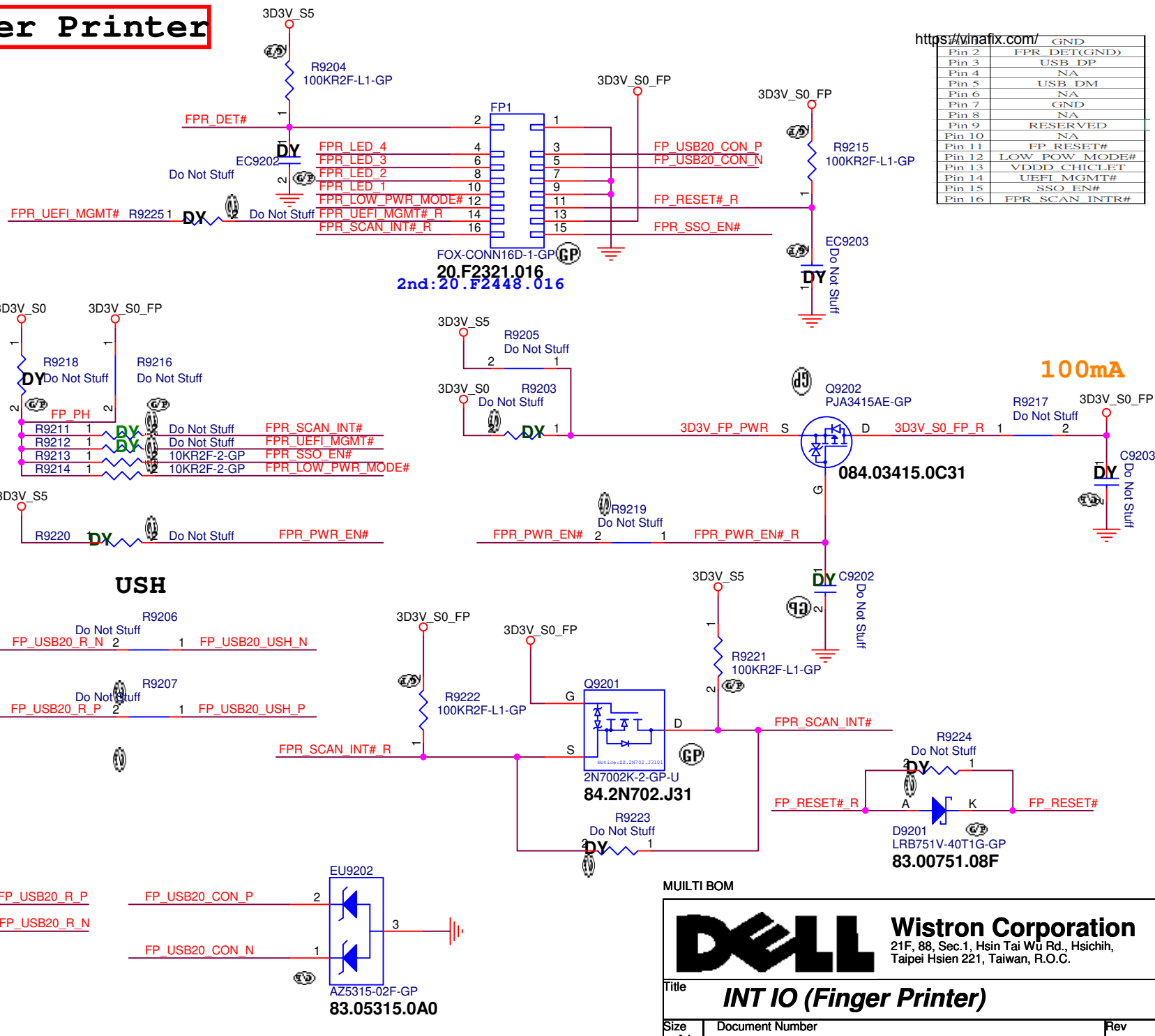
[16] FP_USB20_N <<<—

[64] FPR_LED_1 >>>—

[64] FPR_LED_2 >>>—

[64] FPR_LED_3 >>>—

[64] FPR_LED_4 >>>—



MULTI BOM



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **INT IO (Finger Printer)**

Size A4 Document Number

Rev **A00**

Date: Wednesday, October 28, 2020

Sheet 92 of 106

5

4

3

2

1

<https://vinafix.com/>

D

D

C

C


B

B


A

A

MULTI BOM

			Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title EXT IO (RSVD) (Express Card/PCIE slot)					
Size A4		Document Number			Rev A00
Date: Wednesday, October 28, 2020			Sheet 93 of 106		

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (RSVD) (Smart Card/COM/PS2)		
Size A4	Document Number	Rev A00
Date: Wednesday, October 28, 2020		Sheet 94 of 106

5

4

3

2

1

D

D

C

C


B

B

A

A

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title EXT IO (RSVD) (Docking/LPT)		
Size A4	Document Number	Rev A00
Date: Wednesday, October 28, 2020		Sheet 95 of 106

5

4

3

2

1

<https://vinafix.com/>

D

D

C

C


B

B

A

A

MULTI BOM

 <div>Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>		
Title Commercial (RSVD) (SW GFX eDP)		
Size A4	Document Number	Rev A00
Date: Wednesday, October 28, 2020		Sheet 96 of 106

5

4

3

2

1

<https://vinafix.com/>

D

D

C

C


B

B

A

A

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Commercial (Intel LAN)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 97 of	106

5


4

3

2

1

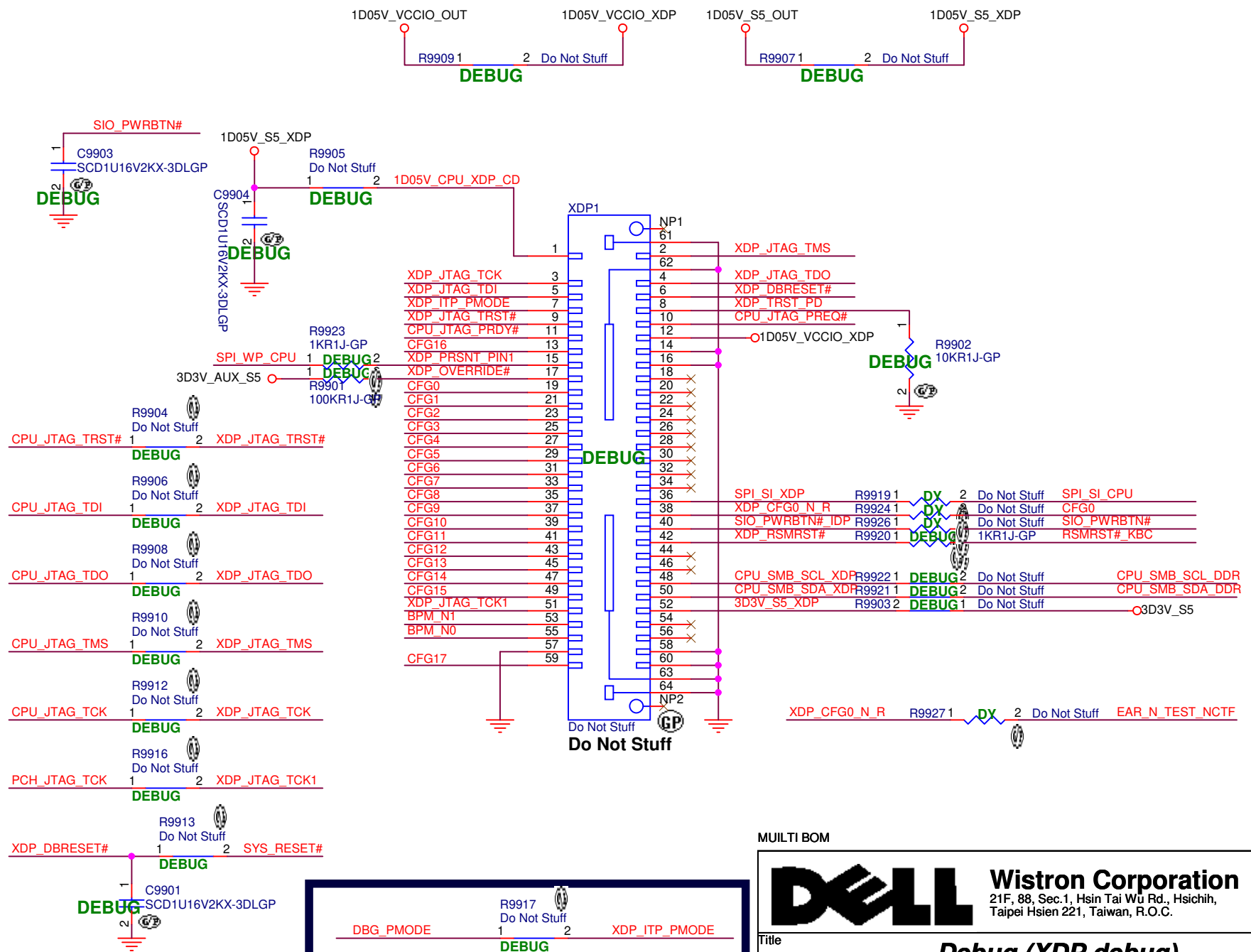
MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Commercial (LAN Switch)			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 98 of	106

Main Func = Debug (MIPI)

https://vinafix.com/

- [6] CFG0 >>>
- [6] CFG1 >>>
- [6] CFG2 >>>
- [6] CFG3 >>>
- [6] CFG4 >>>
- [6] CFG5 >>>
- [6] CFG6 >>>
- [6] CFG7 >>>
- [6] CFG8 >>>
- [6] CFG9 >>>
- [6] CFG10 >>>
- [6] CFG11 >>>
- [6] CFG12 >>>
- [6] CFG13 >>>
- [6] CFG14 >>>
- [6] CFG15 >>>
- [6] CFG16 >>>
- [6] CFG17 >>>
- [6] BPM_N0 >>>
- [6] BPM_N1 >>>
- [3,15] DBG_PMODE >>>
- [3] PCH_JTAG_TCK <<>>
- [3] CPU_JTAG_PRDY#<<>>
- [3] CPU_JTAG_PREQ#<<>>
- [3] CPU_JTAG_TRST#<<>>
- [3] CPU_JTAG_TCK <<>>
- [3] CPU_JTAG_TDI <<>>
- [3] CPU_JTAG_TDO <<>>
- [3] CPU_JTAG_TMS <<>>
- [17,68] SYS_RESET# >>>
- [17,24] SIO_PWRBTN# >>>
- [18] CPU_SMB_SCL_DDR<<>>
- [18] CPU_SMB_SDA_DDR<<>>
- [15,18,68] SPI_SI_CPU <<>>
- [15,18,68] SPI_WP_CPU <<>>
- [17,24,64] RSMRST#_KBC <<<
- [40] XDP_OVERRIDE# <<<
- [3] EAR_N_TEST_NCTF <<>>



DBG_PMODE 1 2 XDP_ITP_PMODE
Do Not Stuff
Pull high on Page15

MULTI BOM

DELL Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: **Debug (XDP debug)**

Size A4	Document Number SouthPeak13 TGL	Rev A00
Date: Wednesday, October 28, 2020		Sheet 99 of 106

Table of Content

<https://vinafix.com/>

RESISTOR

Symbol name	Value	Tolerance (J: 5%, F: 1%, D: 0.5%, B: 0.1 %)	Rating 0402=> 1/16W, 25V 0603 => 1/16W, 75V 0805 => 1/10W, 100V	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
10KR3	10K Ohm	If no letter, it means J: 5%	1/16W, 75V	0603
33D3R5	33.3 Ohm	If no letter, it means J: 5%	1/10W, 100V	0805
1KR3F	1K Ohm	F: 1%	1/16W, 75V	0603

The naming rule is value + R + size + tolerance
 For the value, it can be read by the number before R. (R means resistor)
 For the tolerance, it can be read from the last letter.
 For the rating, we don't show on the symbol name.
 For the size, R2=>0402, R3=>0603, R5=>0805,....

CAPACITOR

Symbol name	Value	Tolerance (M: +/-20, K: +/-10, Z: +80/-20)	Rating	Size 2=>0402, 3=>0603, 5=>0805, 6=>1206, 0=>1210
SCD1U10V2MX-1	0.1uF	M/X5R	10V	0402
SC10U6D3V5MX	10uF	M/X5R	6.3V	0805
SC2D2U16V5ZY	2.2uF	Z/Y5V	16V	0805

The naming rule is
 Capacitor type + value + rating + size + tolerance + material
 SCD1U10V2MX-1
 SC=> SMT Ceramic, TC=> POS cap or SP cap
 D1U => 0.1uF
 10V => the voltage rating is 10V
 2=> 0402, 3=>0603, 5=>0805
 M=>tolerance M, K, Z
 X=> X7R/X5R, Y=> Y5V
 -1 => symbol version, nonsense to EE characteristic

MULTI BOM



Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Table of Content

Size
A4

Document Number

Rev
A00

Date: Wednesday, October 28, 2020

Sheet 100 of 106


Change notes - X02

Item	Page	Issue description	Change item
X01	12	C1243 change 1uF 0201 to 0402 10uF to enhance 1D2V.	C1243 change 1uF 0201 to 0402 10uF
X01	13	Add 24 pcs 0201 1uF cap to enhance 0D6V.	00D6V_VREF_S0 add 0201 1uF cap, 24 pcs
X01	12, 13	Follow PDG v1.2 to change resistor and cap value.	1. Change RN1201, RN1205, RN1202, RN1203, RN1204, RN1206, RN1311, RN1310, RN1308, RN1312, RN1309 to 0201 36R 2. R1214, R1215 ,R1211, R1212, R1324 ,R1319 ,R1317, R1318 change from 39 ohm to 36 ohm(64.36R05.6DL)
X01	15	Follow PDG v1.2 to change strap pin SPI_S1_CPU pull high resistor value.	R1503 change from 100k to 4.7k to follow PDG.
X01	16	Add 2_IN_1_DET# pin to identify 2 in 1 and CS SKU. (Use PCH GPP_E4 and EC GPIO100 connect SENBD1.3, High for CS, Low for 2 in 1)	Set GPP_E4 to 2_IN_1_DET# to connect SENBD1.3, and reserve 0 ohm to GND at sensor board side.
X01	18	Add TPW12 pin to identify 31 and 100VDRON TPM. (Use GPP_E47, High for 31, Low for 100VDRON)	Add netname TPM_ID and pull high, pull down resistor(R1812, R1818) as strap pin.
X01	18	Add Nanya DRAM and add new memory config BOM control.	
X01	24	Board ID change from X00 to X01	Change BOARD_ID PH res R2484 from 240k to 130k.
X01	24	MEC5200 strap pin follow vendor suggestion to modify.	Add BOM control for strap pin ESPI_SHARE_BOOT_SELECT, High for 5107, Low for 5200.
X01	25	Remove RTC connector, Remove BIOS ROM socket.	Set RTC1 to DY, U2501 change from 062.10029.0091 to 072.25256.0L01
X01	26	Based on thermal request to move Q2601 and Q2605 location.	
X01	40	Add RC delay for tPCH04(3D3V_RTC_PCH stable (@90% of full value) to 3D3V_VCCDSW starting to ramp.) sequence fix	Change R4052 from 0 ohm to 100k, add C4034 0.1uF.
X01	43	For using MX battery in DVT1, change BOM control.	Stuff MX_BAT property items(PR4461, Q4302, R4301, R4330), DY BD_BAT items(PC4430, PR4447, R4329).
X01	44, 47, 50	Acoustic cap 100uF change to 68uF(3pcs)	TC4402, TC4702, TC5004 change from 100uF(077.C1071.0071) to 68uF
X01	51	Add 3 gap for VDDQ power plane to enhance VDDQ.	Add PG5120~22
X01	57	For HDMI 2.0 test result to add common choke.	Add EL5702, EL5703, EL5704, EL5705 for HDMI2.0
X01	72	Follow PD controller vendor suggestion to modify schematic.	1. Change C7216, C7215, C7220, C7221 220pf tp 330p(R78.333124.2FLDL) to follow vendor suggestion.
X01	72	1. According to BU comment, if the GATE_VSYS used as GPIO, it should add 330pF to GATE_VSYS pin.	2. Add 330pf to GATE_VSYS.
X01	72	2. When CC pin doesn't add protection(TPD45311), add 330pF at CC1 and CC2.	
X01	72	PD controller(U7201) change to new part number(vendor p/n SN1908005YBGR)	Apply new part number for SN1908005YBGR.
X01	74	Power team suggestion(follow power SA comment) to simplify type-C power circuit.	Stuff: R7424, R7467, R7482, R74014. DY: C7420, C7429, Q7410, Q7414, Q7423, Q7426, R7433, R7439, R7443, R7444, R7449, R7451, R7481, R7483, R7485, R7496, R7497, R74001.
X01	74	Add delay capacitor at DCIN1_EN# and DCIN2_EN# for fix type-C abnormal	Q7417, Q7429 pin 3(DCIN1_EN# and DCIN2_EN#) add 1uF 6.3V cap(C7404, C7405)
X01	91	TPM use AHD4 or AHD8 for DVT1?	AHD8 is obsolete now.
X01	92	Follow latest finger printer vendor spec.	Change finger printer LED resistor to 4.99K(5K)(R6414, R6415, R6416, R6417)
X01	44, 89	Follow RF team suggestion to change BOM.	0402 680pf=78.68124.2FLDL 0402 1000F=78.10224.2FLDL Add EC8901, EC8902 680pf Add EC8903, EC8904 1000pf Change FC4408 from 1uF to 680pf Change FC8911 from 1uF to 680pf Change FC4410 from 1uF to 680pf Change FC8913 from 1uF to 680pf Change FC8904 from 1uF to 680pf Change FC8914 from 1uF to 680pf Change FC8905 from 1uF to 680pf Change FC8915 from 1uF to 680pf Change FC8906 from 1uF to 680pf Change EC8924 from 1uF to 680pf Change FC8907 from 1uF to 680pf Change EC8970 from 1uF to 680pf Change FC8910 from 1uF to 680pf Change FC4507 from 1uF to 1000pf Change FC4409 from 1uF to 1000pf Change EC8907 from 1uF to 1000pf Change PC5105 ~ PC5101 ~ PC5302 ~ PC5313 to 0603 size
X01	51, 53	Power team circuit modify.	Change PC5105 ~ PC5101 ~ PC5302 ~ PC5313 to 0603 size
X01	Multi ple	Follow connector list.	

Item	Page	Issue description	Change item
X02	5	Add property on ED502 SM_DRAMRST#_CPU TVS on Memory 32G config unstuff for IRMT test result is improve.	1.Set TVS ED502 to 32GB only, but 4GB/8GB/16Gb still stuff. Since EMC already verify pass.
X02	12, 13	Follow TGL latest PDG.	1. DDR_ALERT# disconnect to CPU.
X02	12, 13	Change DDR resistor size for layout space.	1. R1209, R1210, R1341, R1342 change to 0201 size.
X02	20	Follow intel suggestion to change ISH related pull high resistor from 100K to 10K to make stronger.	1. R2039, R2040 from 100K to 10k ohms .
X02	22	Change Q2201 B gate from 3D3C_S5_PCH to 1D05V_VCCSTG_TERM prevent VRALERT# assert to abnormal voltage .	1. Add R2203 connect to 1D05V_VCCSTG_TERM . 2. Dummy R2202 .
X02	24	Correct Top swap connection .	1. Add R24020 from TOP_SWAP_EN connect to SPKR . 2. Remove R1714 .
X02	24	Change board ID resistor to X02 value.	1. Change R2484 from 130K to 33K ohm.
X02	43	Add extra circuit for improve advance storage mode press once power button boot up.	1. Add Q4304 ,R4309,C4302 .
X02	44	Change charger sense resistor for vendor have abnormal resistor value issue .	1. PR4401 change to 064.R0105.M014.
X02	44, 47, 50, 89	Improve eDP cable routing for ME .	1. Remove TC4402 and CLP37. 2. TC4702 and TC5004 from 68uF to 100uF .
X02	55	Follow connector list to change eDP connector .	1. Change LCD1 to 020.F1829.M001.
X02	56	CHICONY 101mm camera P-sensor detect is NC issue , change MB camera connector pin define.	1. Change CIR1 pin define to meet camera vendor pin define.
X02	62	Dummy WWAN glue logic in DVT2.	1. Add WWAN glue logic related property for BOM control gule logic .
X02	62	Remove reserve UIM_DET reserve pull location , WWAN card have internal pull high .	1. Remove R6258.
X02	64	Reserve EE solution for fix PWRBT EMI test fail issue .	1. Reserve D6401 .
X02	64	Change M_BIST pull high value to prevent abnormal trigger M_BIST .	1. Change R6403 to 1M .
X02	72	Follow vendor suggest to stuff PD TVS.	1. Stuff D7201, D7202.
X02	74	Add Schottky diodes to on MOS S2/S5 to prevent voltage low to charger can't boot up system.	1. Add D7415, D7416 .
X02	91	TPM change to AHD8 to follow latest config.	1. U9101 change to 071.33232.0L03.
X02	72	Change to ROM Less design .	1.Dummy R7268/U7202/C7210/R7250/R2749 .
X02	12	Add more cap to enhance DDR4 power .	1. Stuff C1280, C1281, C1383.
X02	44, 74	OVP Circuit R/C value fine tune .	1. PR4451 change 49.9K to 46.4k ohm 1. Change C7412 and C7428 from 100pf 0201 to 10uf 0402.
X02	64	Fine tune power button brightness .	1. R6404 change 1K to 560k ohms

https://vinafix.com/
Change item

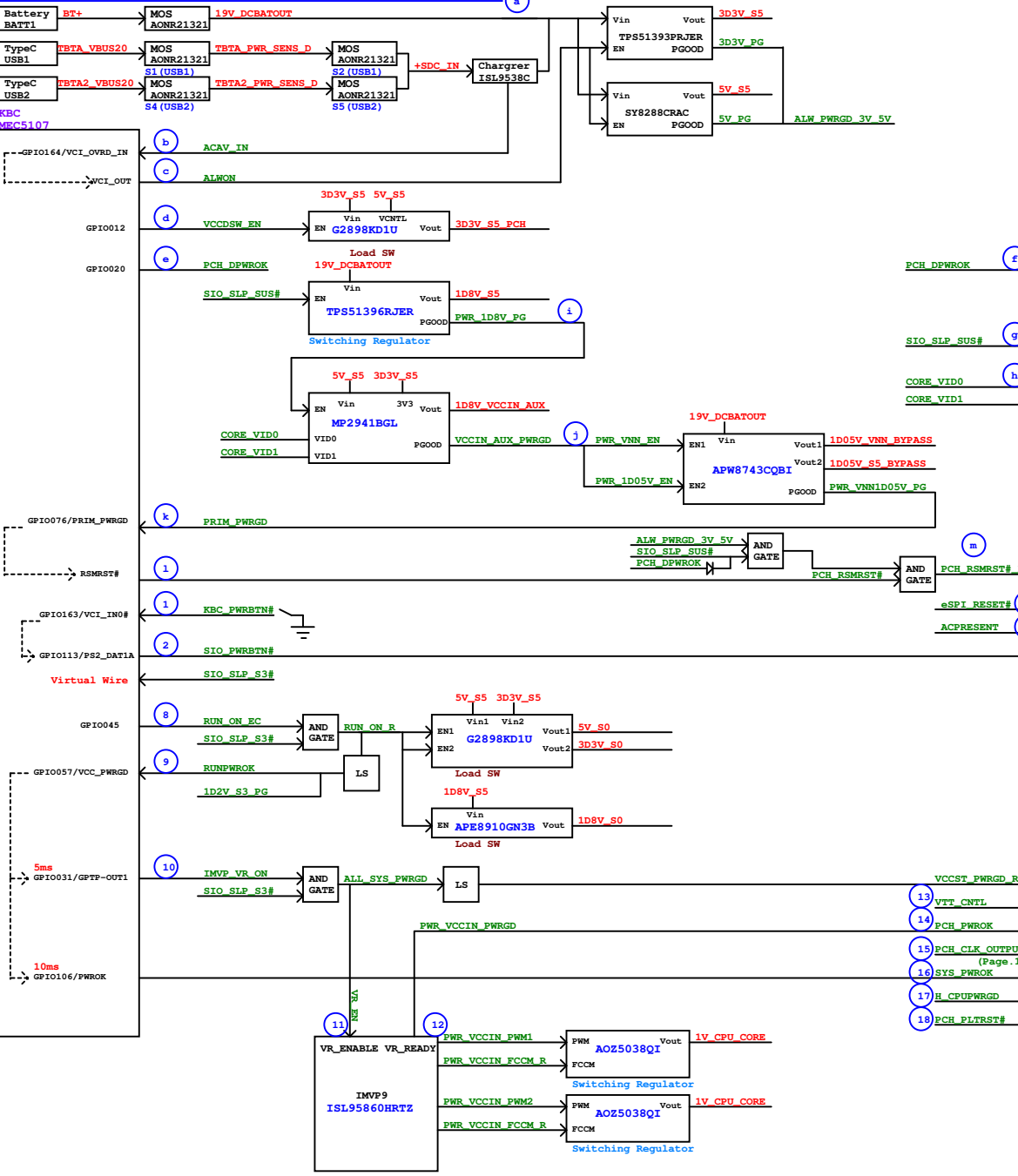
MULTI BOM

**Wistron Corporation**
21F, 8R, Sec.1, Hsin Tai Wu Rd., Hsuehshui, Taipei Hsien 221, Taiwan, R.O.C.

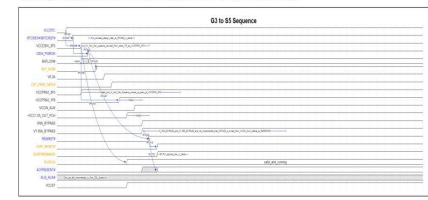
Change History

Title		Rev
Size A2	Document Number	A00
Date: Wednesday, October 28, 2020	Sheet 101	of 108

Southpeak13 Power Up Sequence Diagram (Non_Deep Sx Platform)

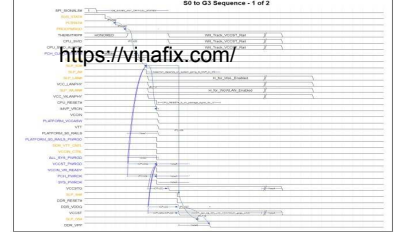


Timing Diagram for G3 to S0 [Non-Deep Sx Platform]



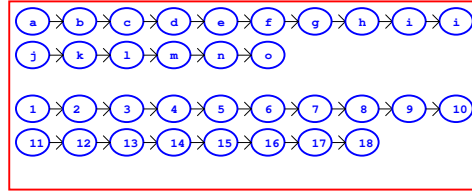
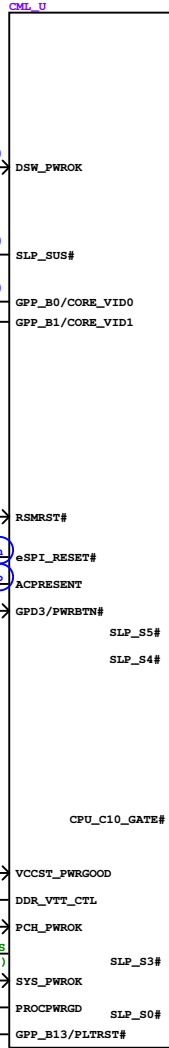
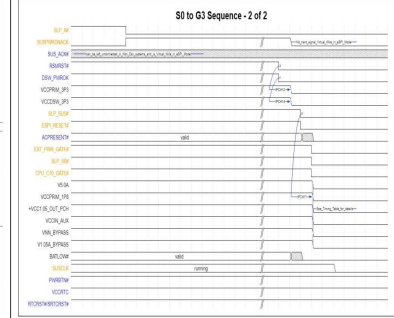
S5 to S0 sequence is same as DSx Sequence (refer to DSx S5-S0 sequence diagram).

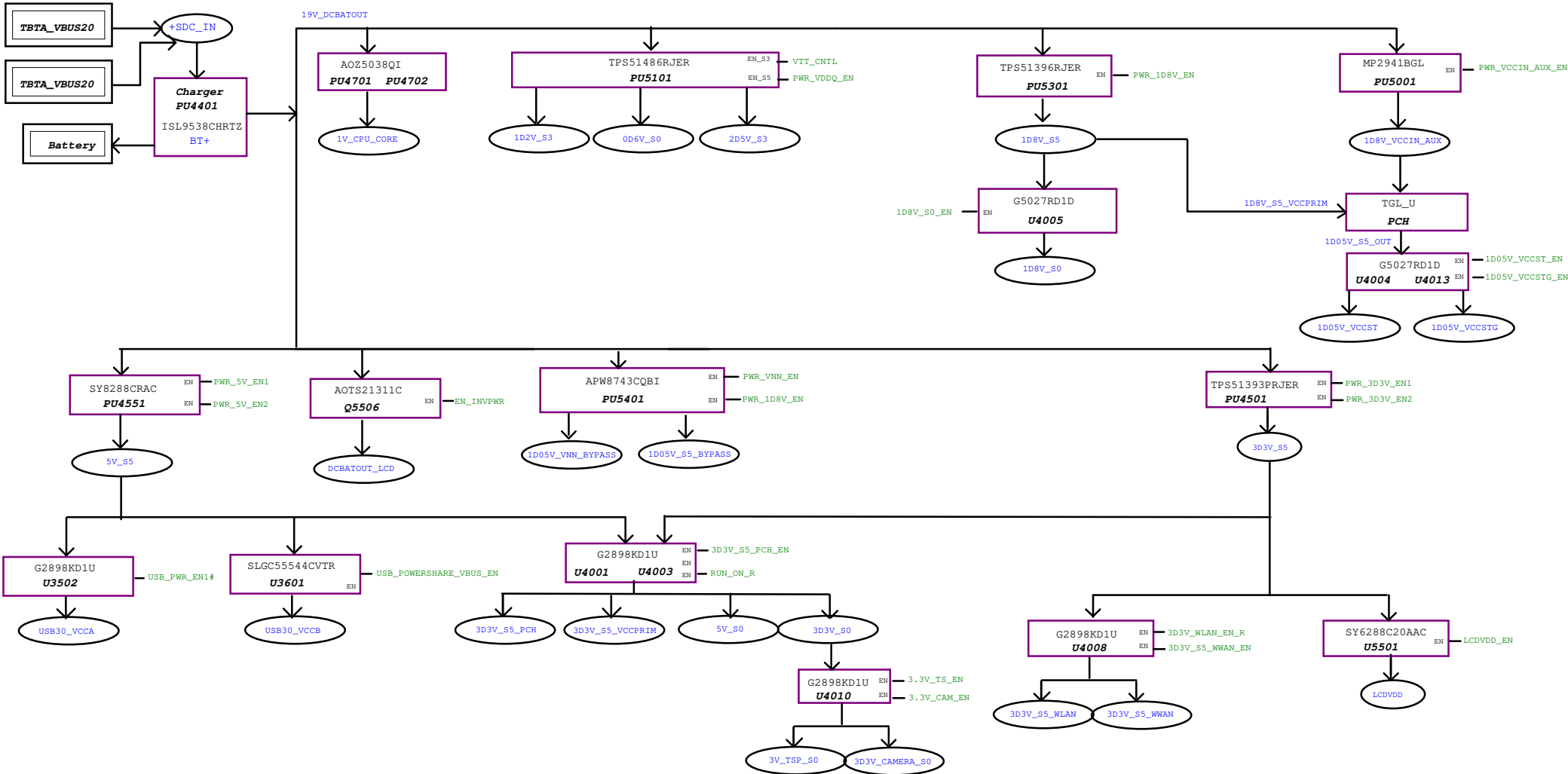
Timing Diagram for S0/M0 to G3 [Deep Sx Platform]



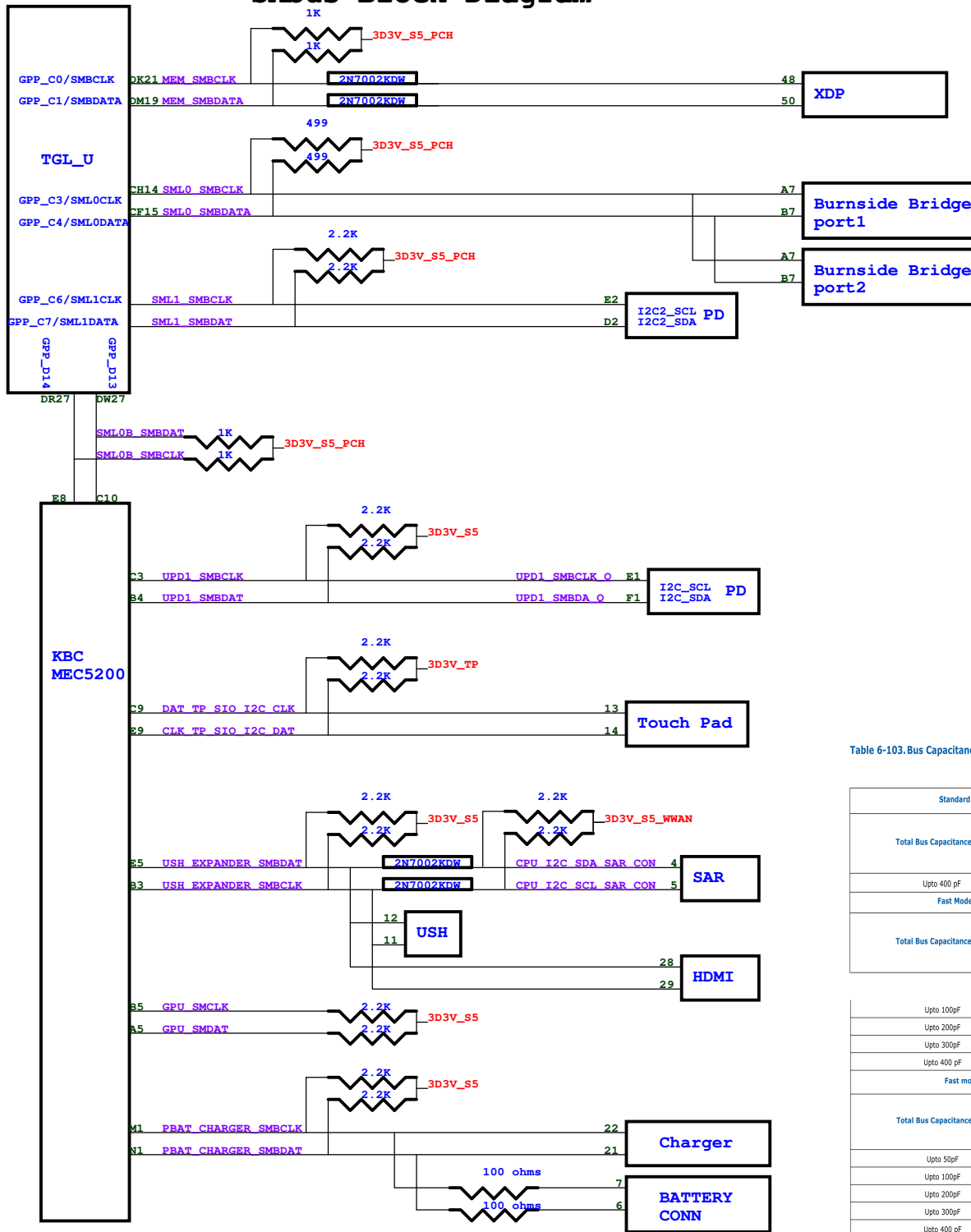
Timing Diagram for S0/M0 to G3 [Non Deep Sx Platform]

For S0 to G3 Sequence 1 of 2 Refer to DSx Sequence





SMBus Block Diagram



I2C Block Diagram

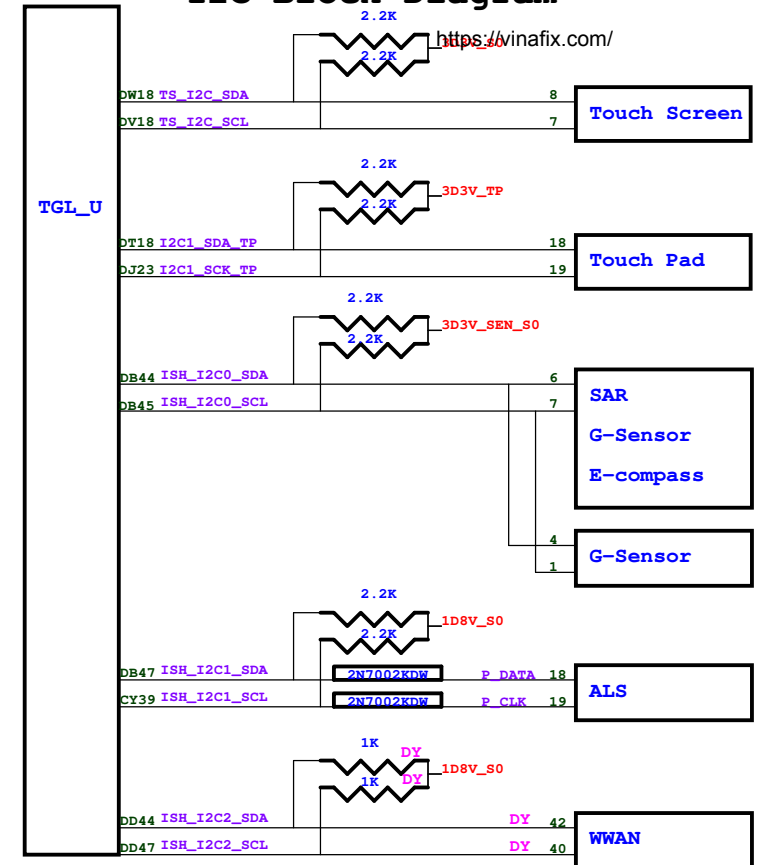


Table 6-103. Bus Capacitance/Pull-Up Resistor Relationship

Standard Mode (100kHz) - Pull-up / Pull-down Resistor Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength (Refer EDS)
Upto 400 pF	2.2KΩ	100Ω
Fast Mode (400kHz) - Mode Pull-up/ Pull-down Strength Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength

Upto 100pF	2.7KΩ	100Ω
Upto 200pF	1.5KΩ	
Upto 300pF	1KΩ	
Upto 400 pF	680Ω	
Fast mode Plus (1MHz) - Pull-up/Pull-down strength Settings		
Total Bus Capacitance (C _b)	External Pull-up	PCH Pull Down Strength
Upto 50pF	2.2KΩ	100Ω
Upto 100pF	1.2KΩ	
Upto 200pF	560Ω	
Upto 300pF	390Ω	
Upto 400 pF	270Ω	67Ω

MULTI BOM

Wistron Corporation
 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

SMBUS/I2C BLOCK DIAGRAM

Title: **SMBUS/I2C BLOCK DIAGRAM**

Size: A3

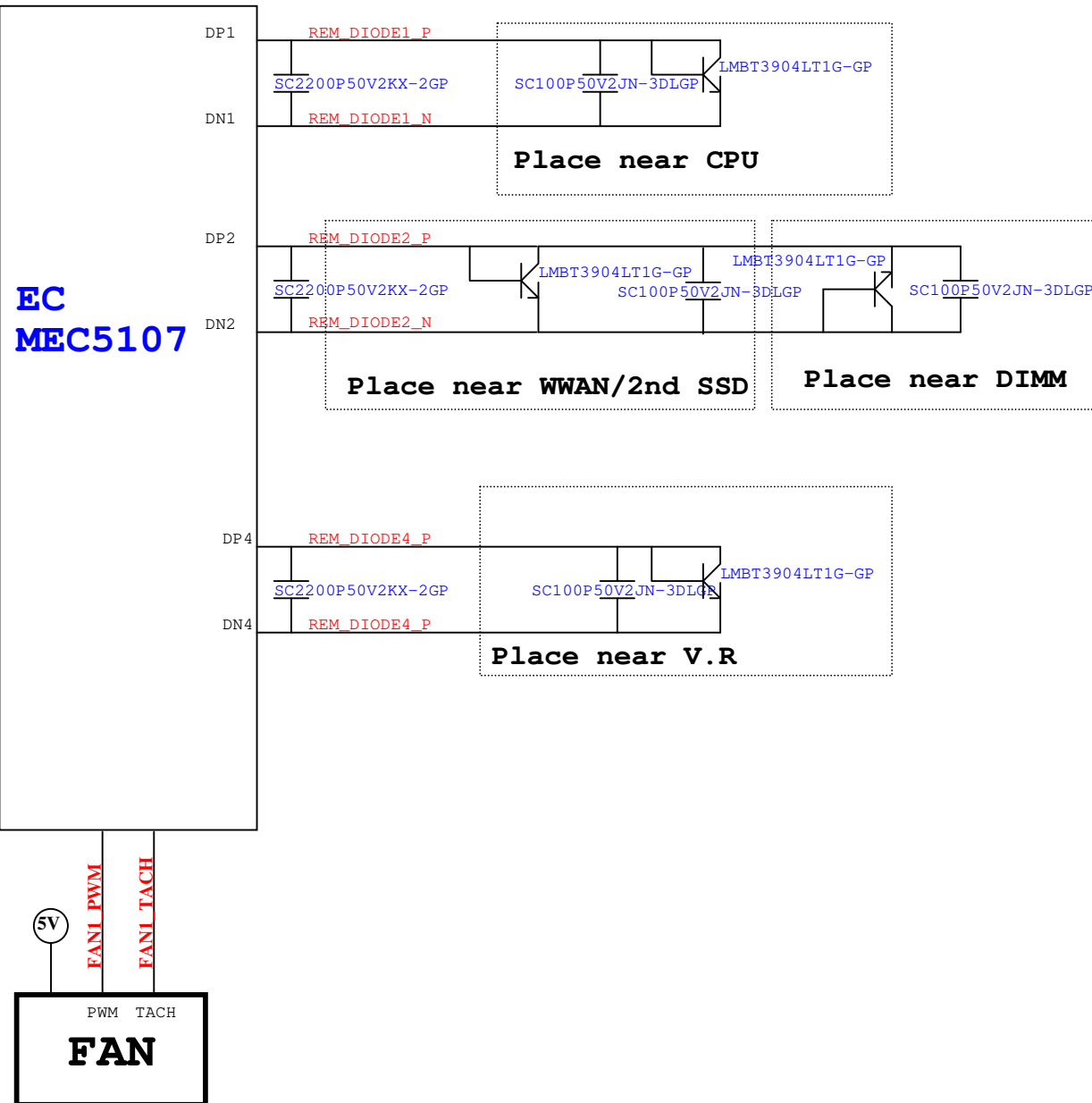
Document Number:

Date: Wednesday, October 28, 2020

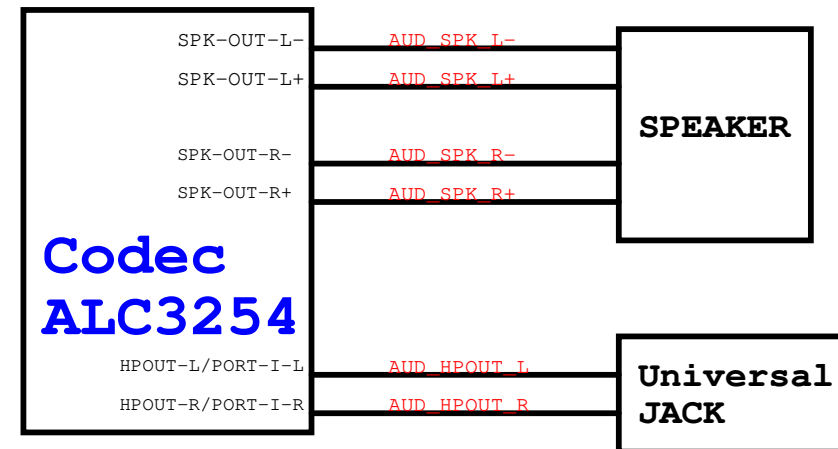
Sheet: 104 of 106

Rev: **A00**

Thermal Block Diagram



Audio Block Diagram



MULTI BOM



Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
THERMAL/AUDIO BLOCK DIAGRAM

Size A4	Document Number	Rev A00
------------	-----------------	-------------------

Date: Wednesday, October 28, 2020 Sheet 105 of 106

5

4

3

2

1

D

D

C

C


B

B

A

A

MULTI BOM

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title CLK Block			
Size A4	Document Number		Rev A00
Date: Wednesday, October 28, 2020		Sheet 106 of	106

5

4

3

2

1